

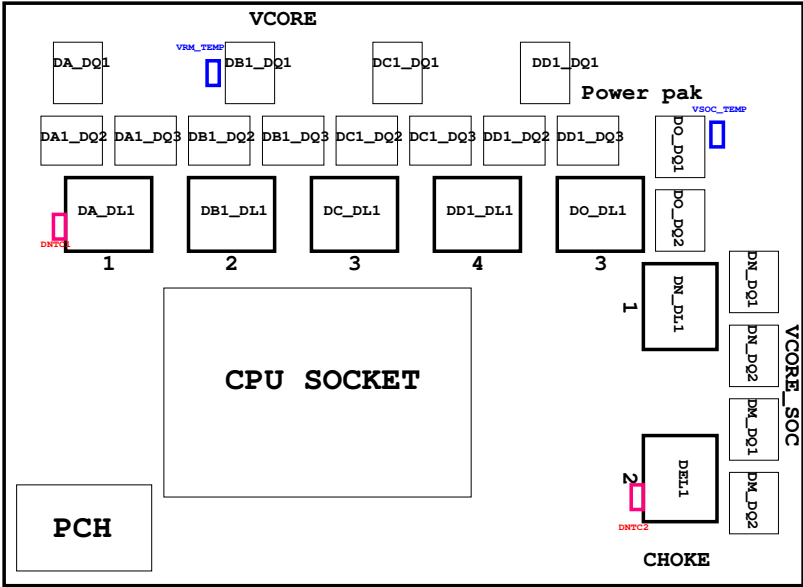
A520M S2H

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GIGABYTETM

Title

COVER SHEET

Size

Document Number

Rev

Custom

A520M S2H

1.11

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Thursday, February 18, 2021

Sheet

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20200210_1410

Model Name: A520M S2H

Component value change history

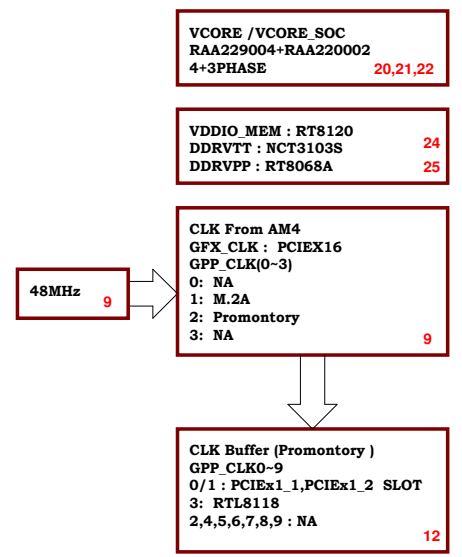
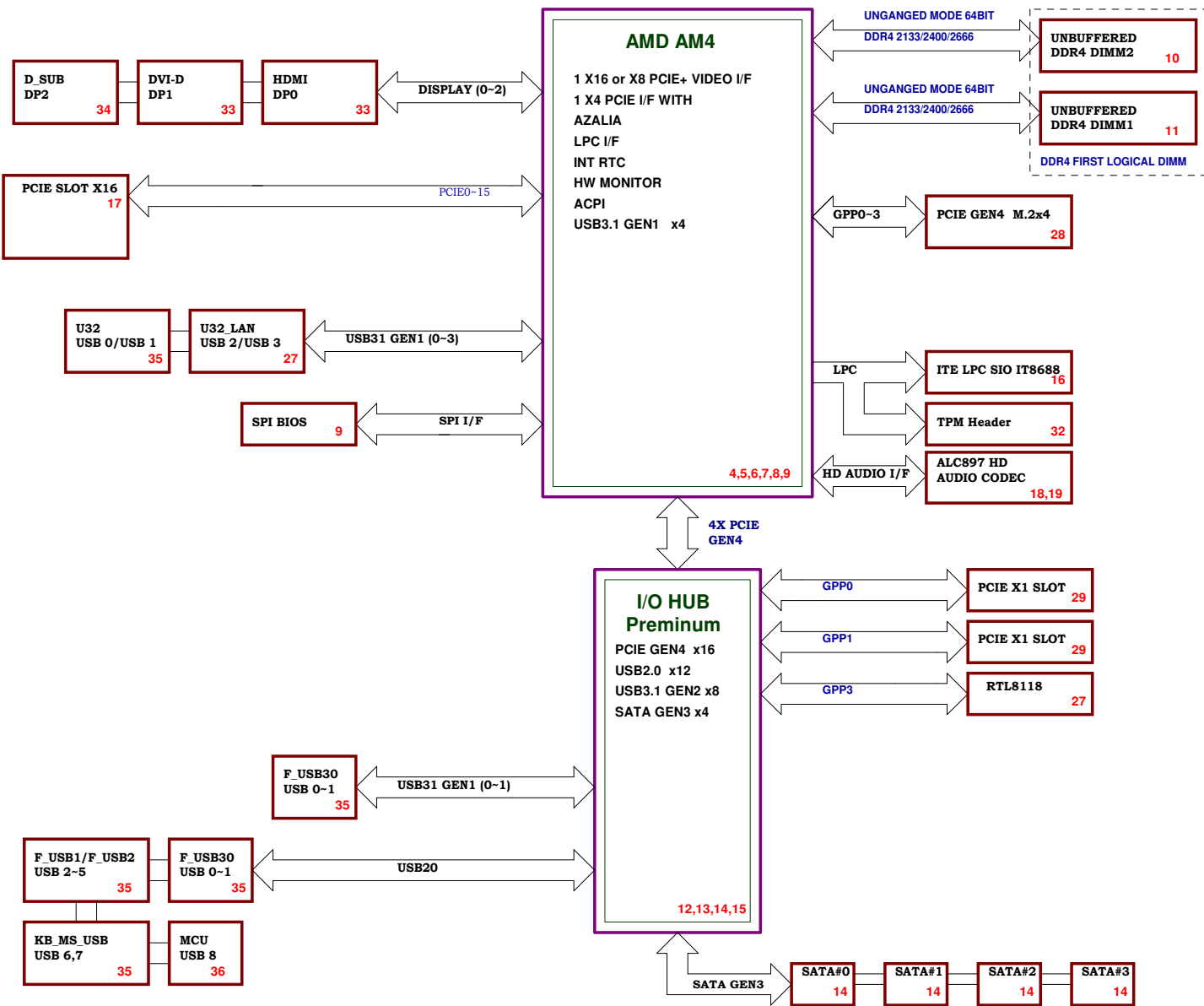
Version: 1.11

P-Code: U98126-0

Date	Change Item	Reason
2020/03/17	Modify from B550M H Rev0.1	
2020/04/24	A520M S2H Rev0.1 First release	
	9MA52MS2H-00-01 BOM	
	9MA52MS2H-00-10A BOM	
2020/05/20	1. Add AR8, ECR5, ECQ4, A_Q7->X 2. DR3, DR10	
	, DR49, DR45, DR41, DR38, DR37, DR5->4. 87K	
	3. U1->10HB1-06A520-10R 4. TPM1->10TA1-E19670-30R	
	5. 80A->12KS2-110202-01R , 12KSF-F10303-01R	
	6. AM4->CPU-SK/1331/BK/S/GF	
	7. M_BIOS->10SL2-000008-71R/X 8. PCIE_X16->11AC1-023164-W2R	
	9. ECD_Q4 上件, ECD_Q5->X 10. DU1->10TA1-622904-06R	
	9MA52MS2H-00-10B BOM	
2020/05/26	1. VSOC_TEMP->10K/1/4/S	
	9MA52MS2H-00-10C BOM	
2020/05/29	1. AR39, AR40->499/4/1	
	9MA52MS2H-00-10E BOM	
2020/05/28	1. 80A->12KSF-F10303-01R , SDO/M3/UD5.5/BD4.0/H0.6/SN	
	2. QFLASH_PLUS->11NR8-050004-02R_11NR8-050004-01R	
	3. AQ2, AR128->X 4. VSOC_TEMP->10K/1/4/S	
	9MA52MS2H-00-10F BOM	
2020/07/30	1. AC26, AC27->150p/4/NPO/50V/J	
	9MA52MS2H-00-10G BOM	
2020/12/23	1. PR76->10K/4/1 , PBC20->1u/4/X5R/6.3V/K	
	9MA52MS2H-00-11A BOM	
2021/01/15	1. ALC897-3+2	
	9MA52MS2H-00-11B BOM	
2021/02/04	1. DU1->10TA1-622904-28R	
	2. AM4->10SC1-P01331-21R/23R	
	9MA52MS2H-00-11F BOM	
2021/02/19	1. PCB Rev1.11	

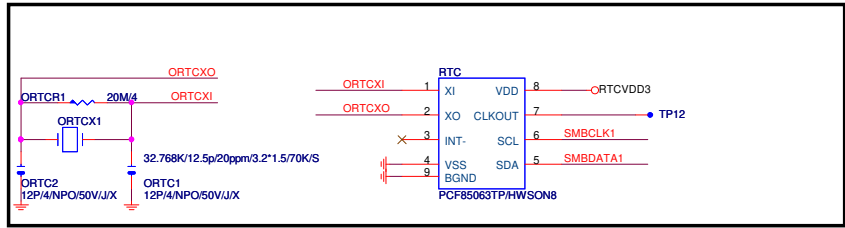
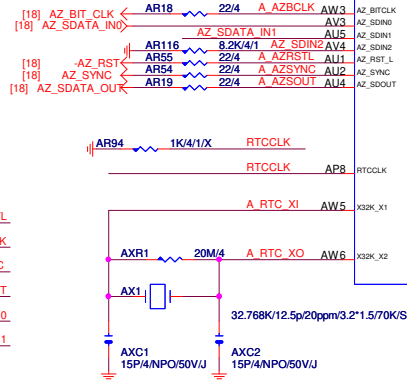
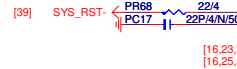
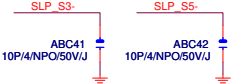
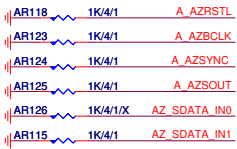
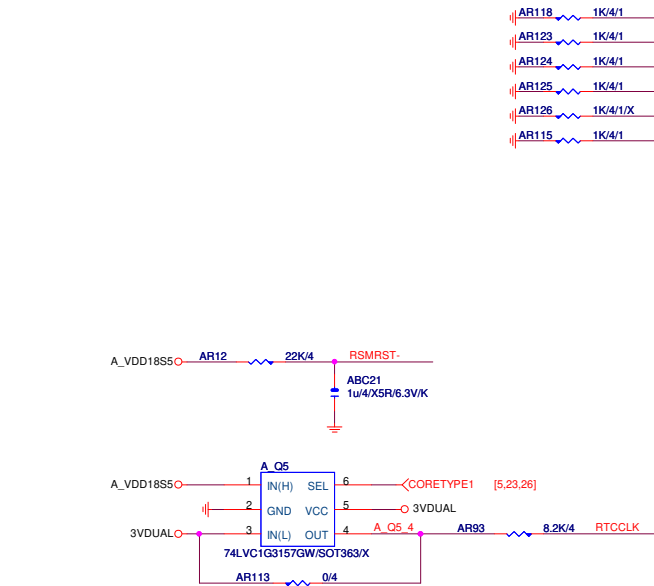
Circuit or PCB layout change for next version

[illegible]

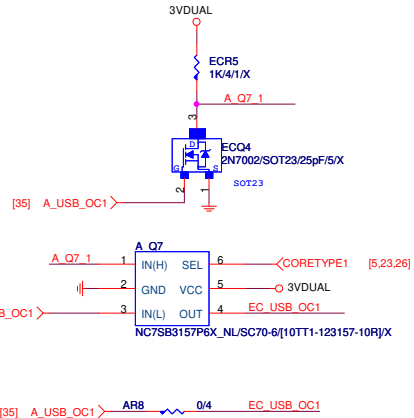
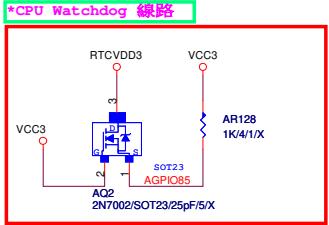
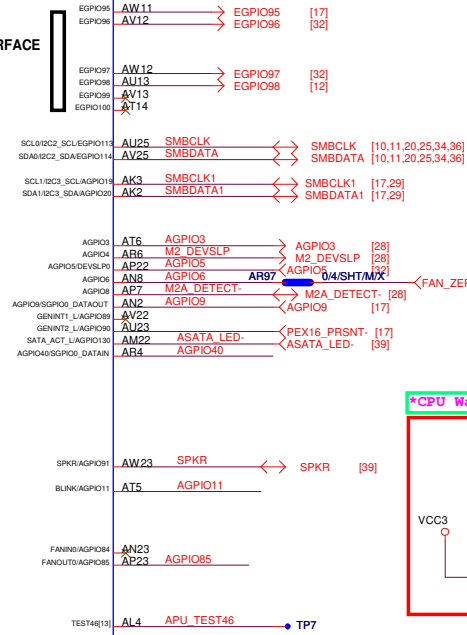


Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

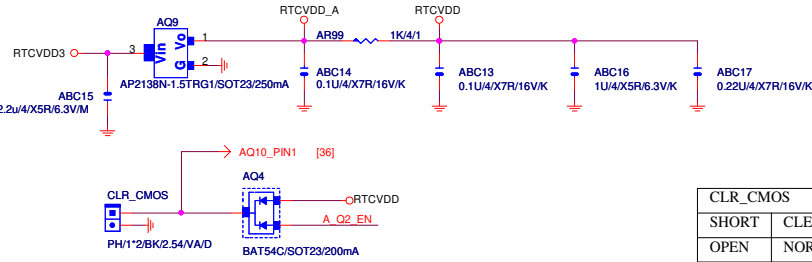
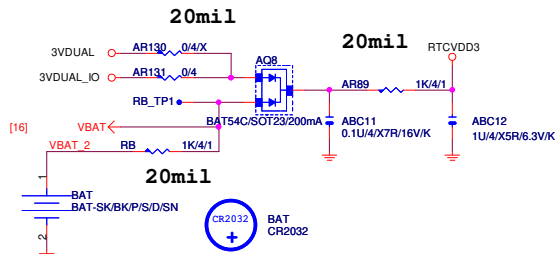
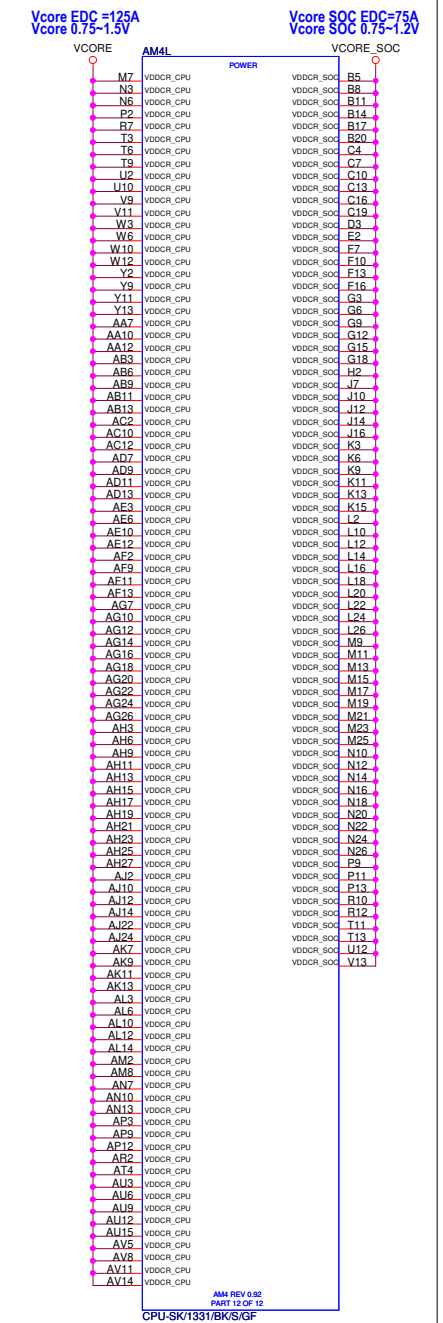
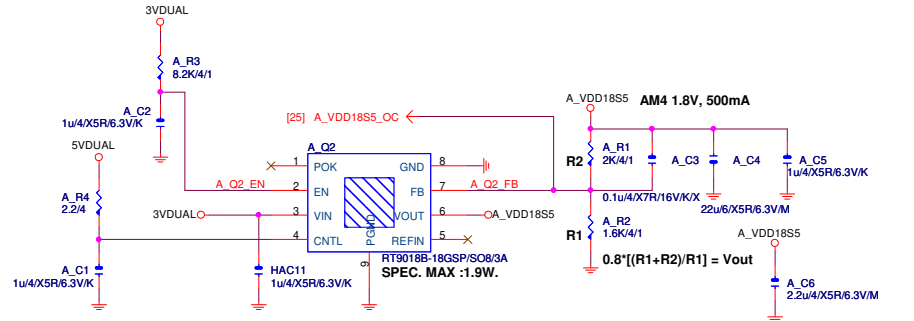
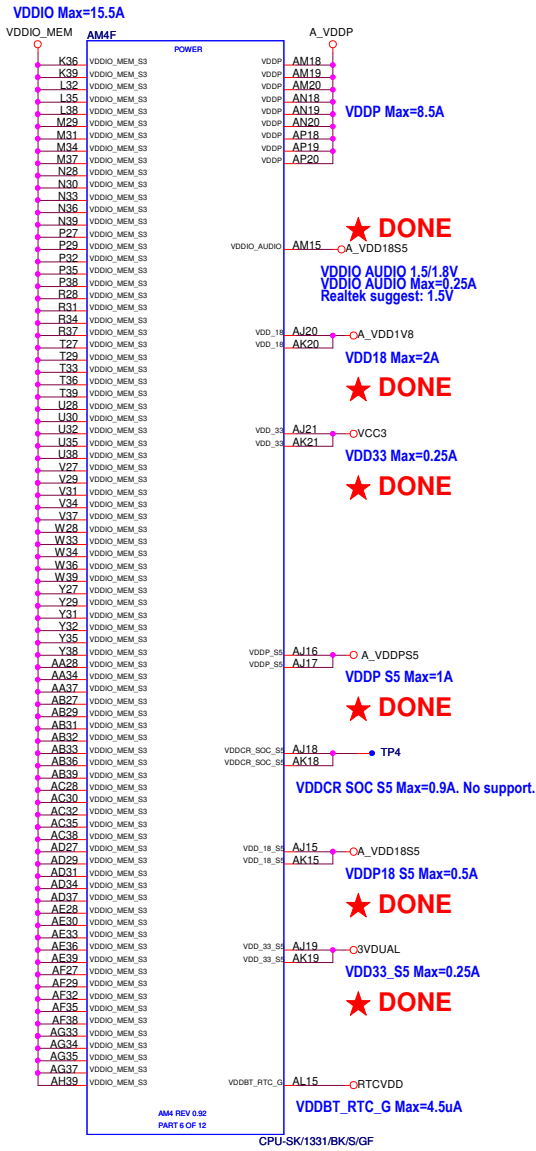


SD INTERFACE



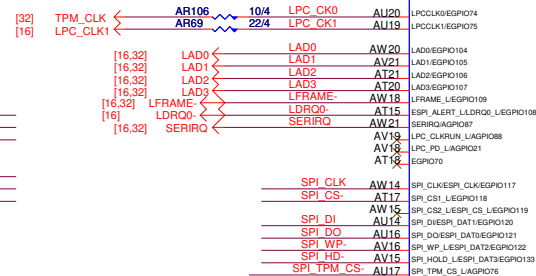
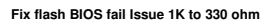
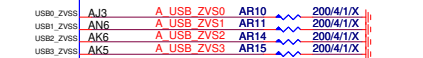
GIGABYTE™

Title			AM4 MISC
Size	Document Number	Rev	1.11
Custom	A520M S2H		
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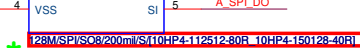


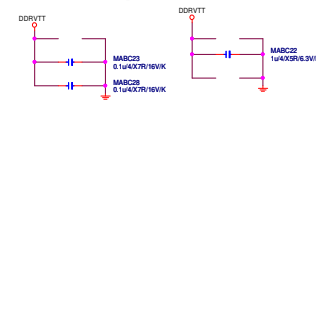
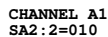
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	

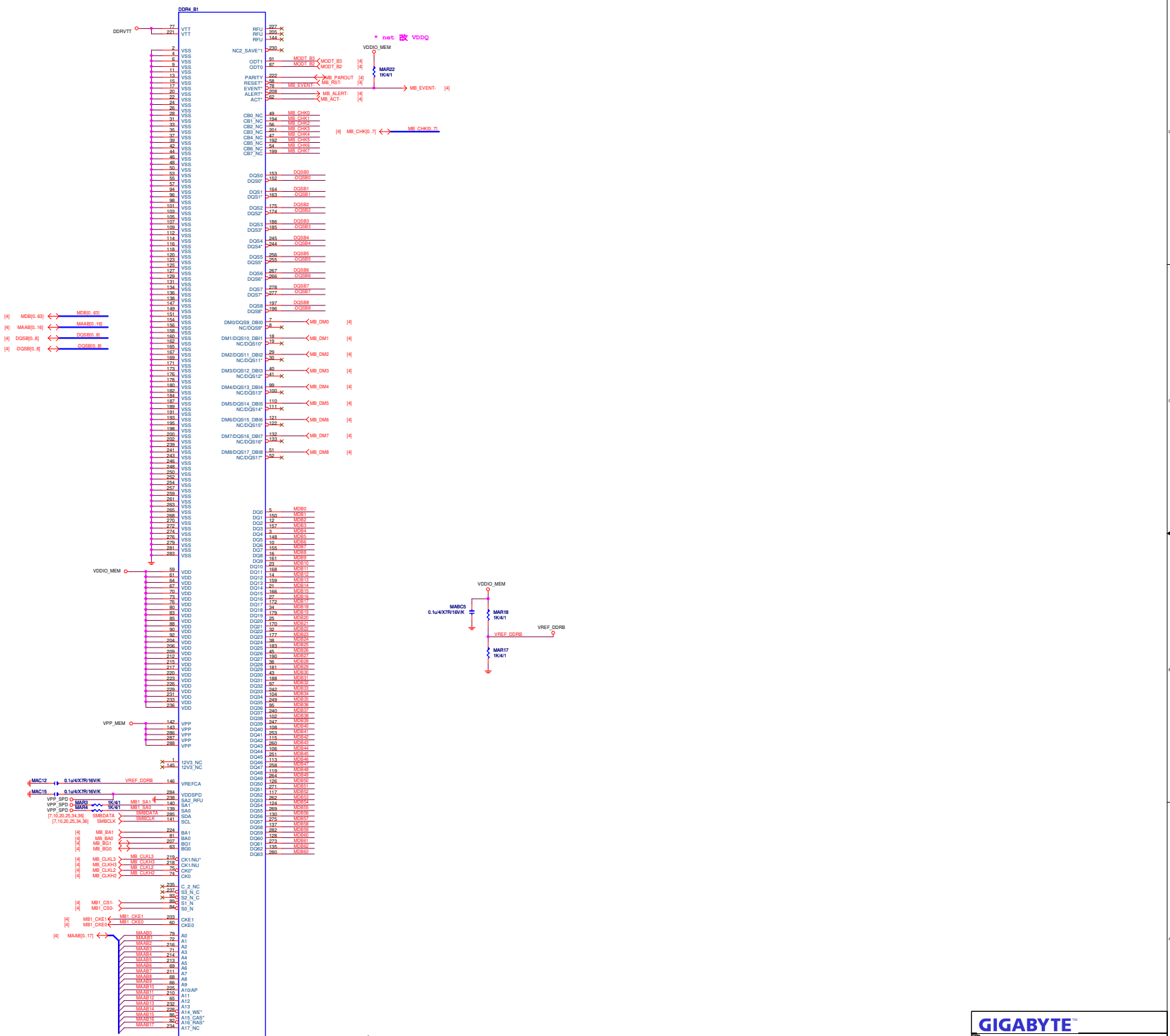
GIGABYTE™			
Title CPU POWER & GND			
Size	Document Number	Rev	
Custom	A520M S2H	1.11	
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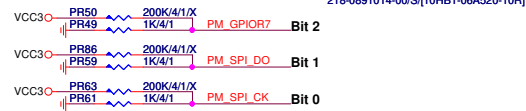
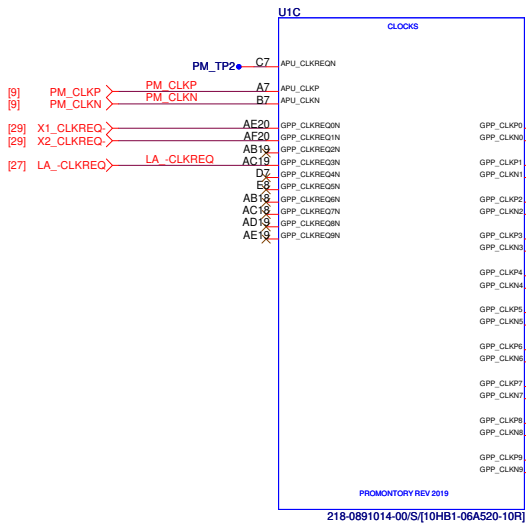
TPM1
SLB9670VQ2.0/VQFN32/S[10TA1-E19670-30R]/X
Footprint : IC32QFN-MASK



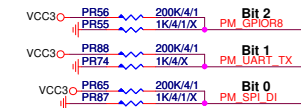




CHANNEL B1
SA2:3=011



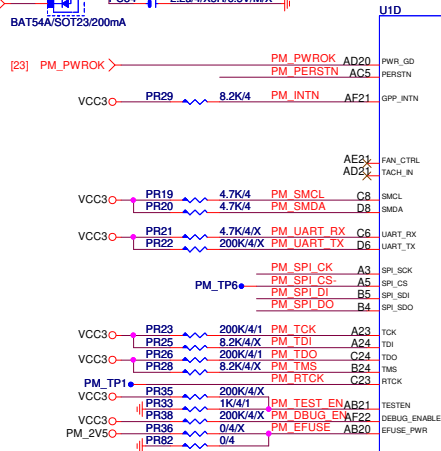
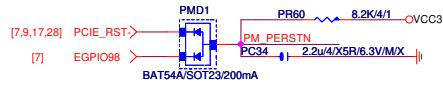
Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



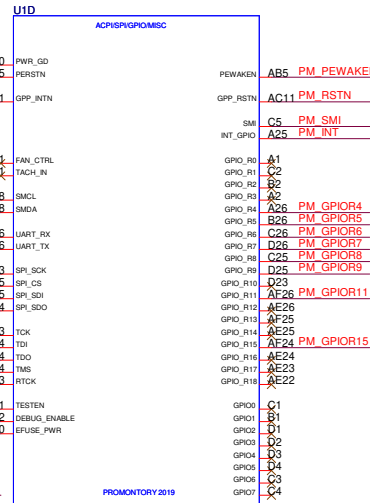
Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



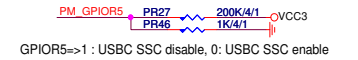
GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1



PR71 1K/4/1 PM_DEBUG_EN
PR79 1K/4/X PM_TCK
PR80 1K/4/X PM_TDO
TESTEN=>1:Test Mode, 0:Function mode.
DEBUG=>1:Debug Mode, 0:Function mode.



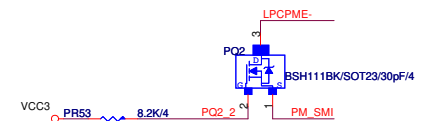
PM_GPIOR4: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.



GPIOR5=>1: USB SSC disable, 0: USB SSC enable

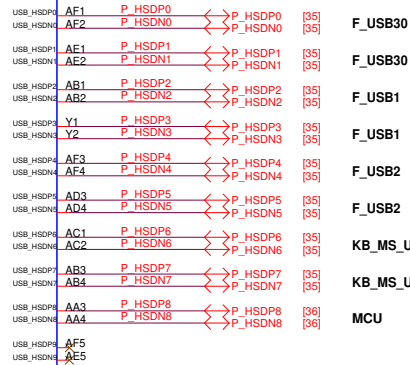
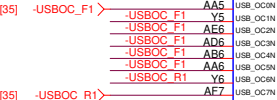


GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable



GIGABYTE™				ANS 8671308
Title				
PROMONTORY CPU/CLK/MISC				
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USB port power control 9:0
(VCC3). Output.



F_USB30

F_USB30

F_USB1

F_USB1

F_USB2

F_USB2

KB_MS_USB

KB_MS_USB

MCU

USB 3.1 Gen 2

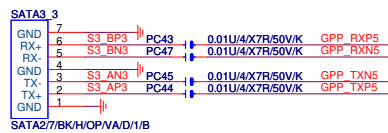
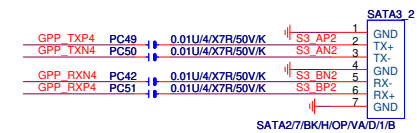
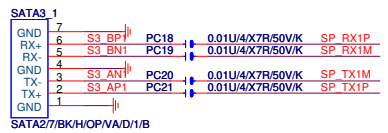
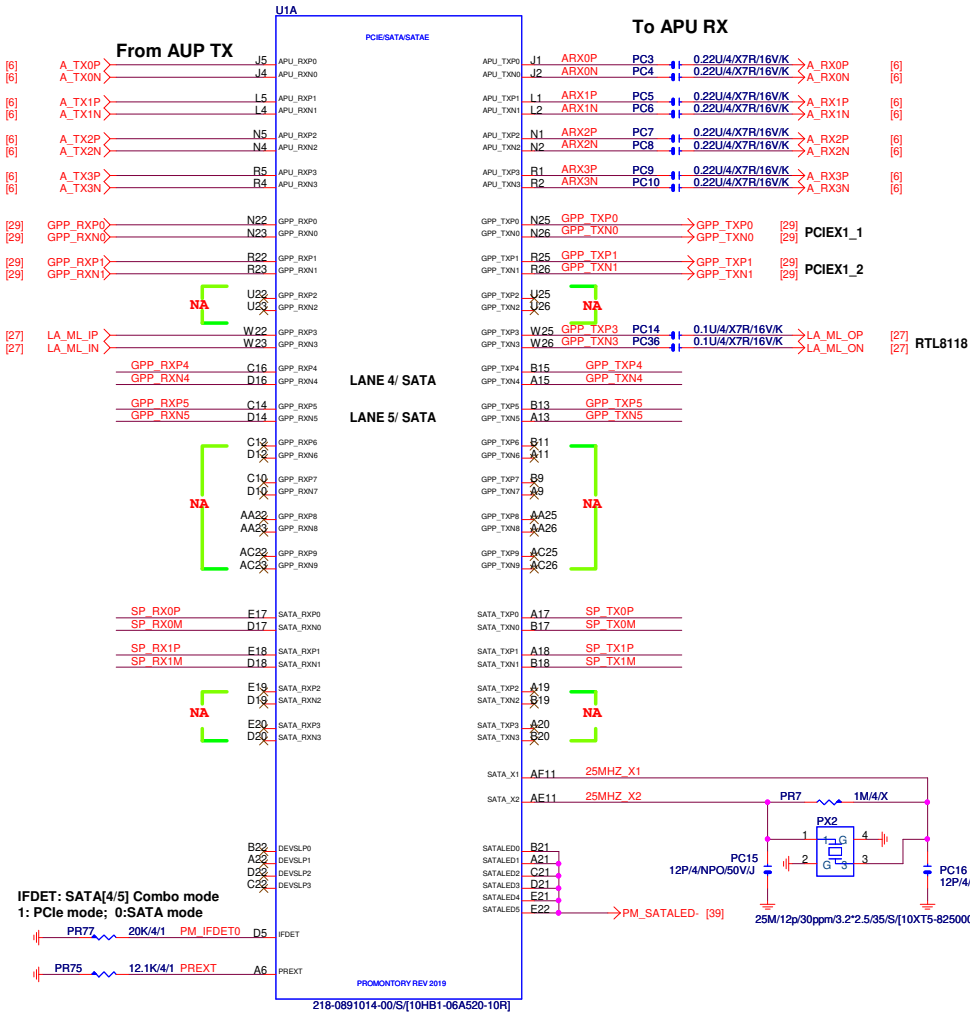


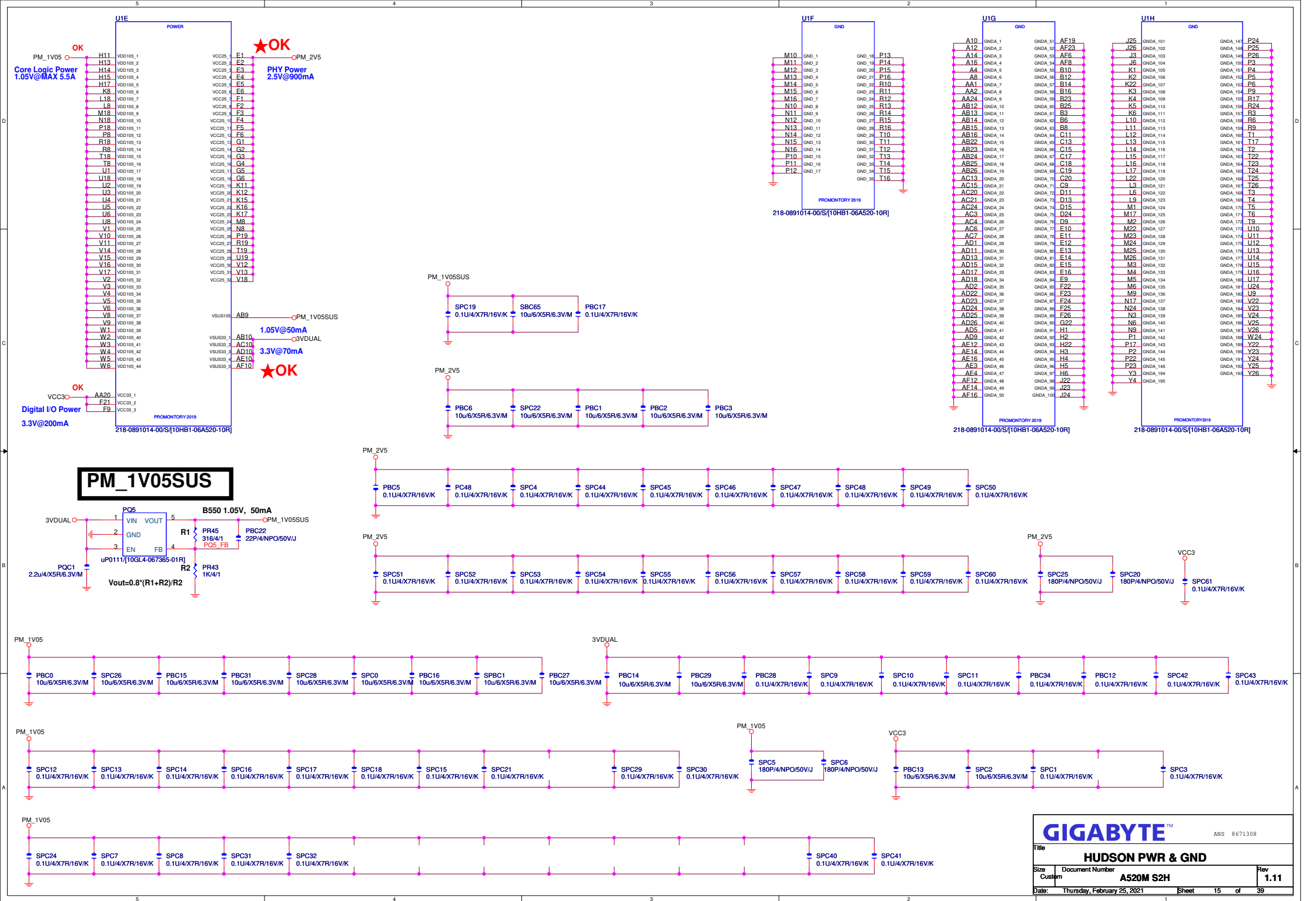
F_USB30

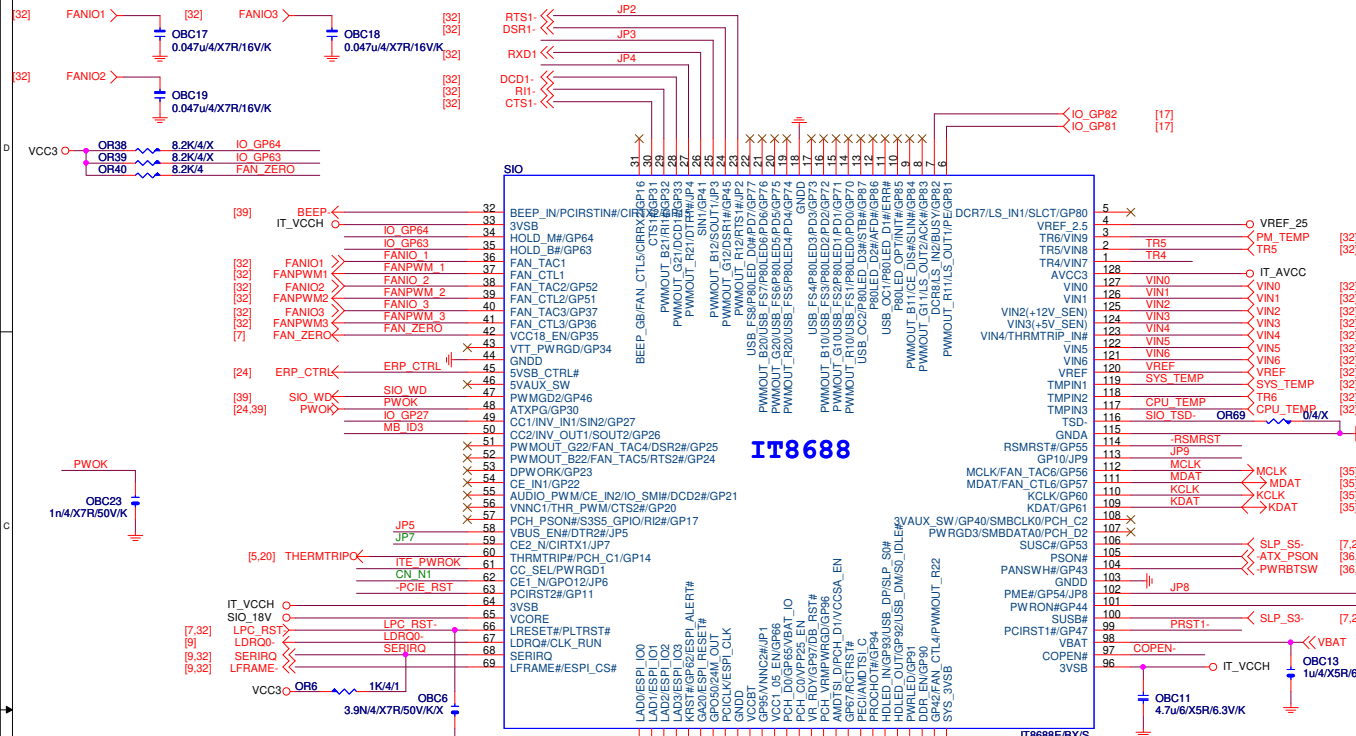
F_USB30

PROMOTORY REV 2019
218-0891014-00/S[10HB1-06A520-10R]

USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

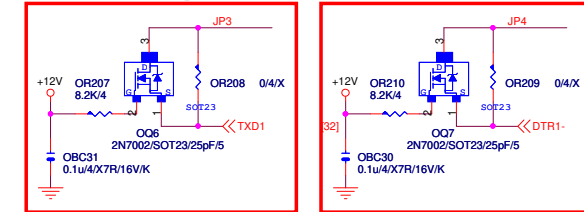




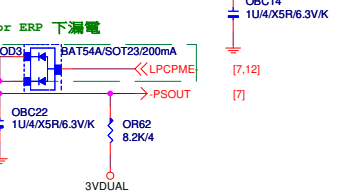
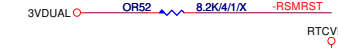


IT8688

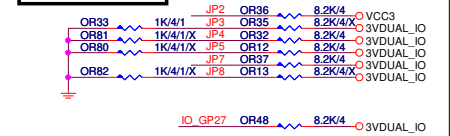
for LPC/eSPI power mode



THROM SPARE GPIO



SIO STRAP



JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/eSPI power VCCBT = 3.3V
	0	LPC/eSPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

MB ID



MB ID2 / Default L/L



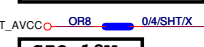
FAN TABLE

CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

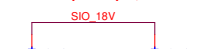
DUAL BIOS OPT STRAP



Power leakage



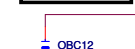
SIO_18V



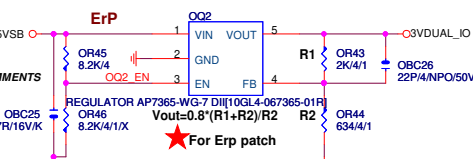
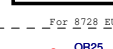
EMI



SIO CAP



PWR SHT



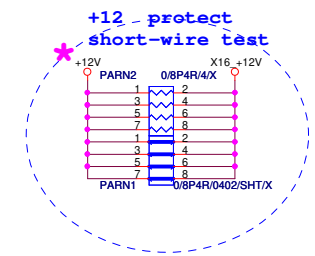
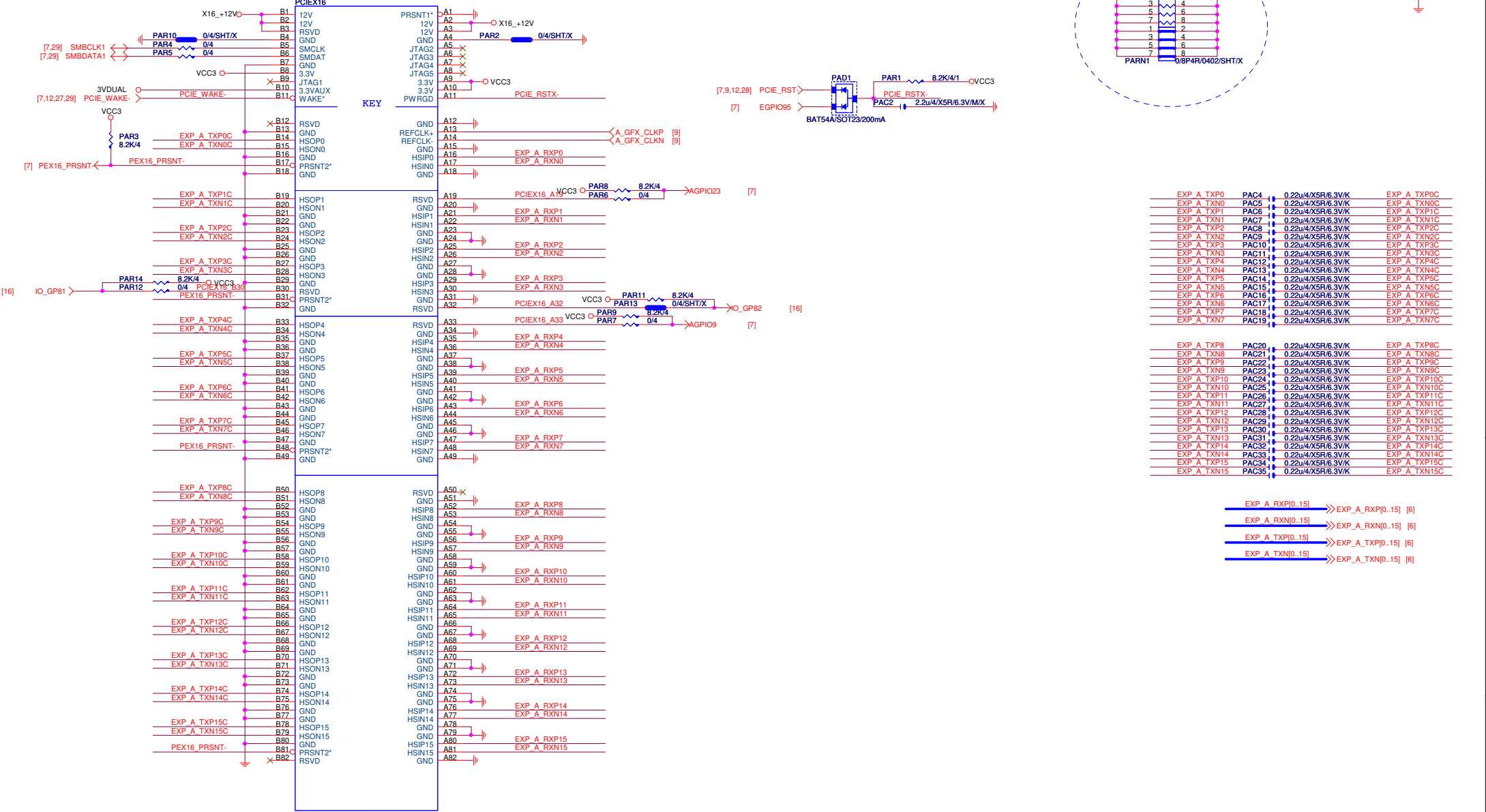
SIO PU



CLOSE SIO PIN4 2_5LEVEL

★ Footprint : PCIESLOT-164P

3GIO_*16

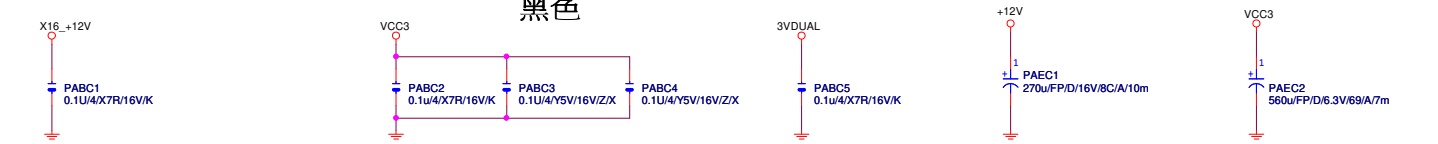


EXP A TXP0	PAC4	0.22u4/X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u4/X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u4/X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u4/X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u4/X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u4/X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u4/X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u4/X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u4/X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u4/X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u4/X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u4/X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u4/X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u4/X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u4/X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u4/X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u4/X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u4/X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u4/X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u4/X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u4/X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u4/X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u4/X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u4/X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u4/X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u4/X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u4/X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u4/X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u4/X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u4/X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u4/X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u4/X5R6.3V/K	EXP A TXN15C

EXP A RXP0.15	>>>EXP_A_RXP0.15	[6]
EXP A RXN0.15	>>>EXP_A_RXN0.15	[6]
EXP A TXP0.15	>>>EXP_A_TXP0.15	[6]
EXP A TXN0.15	>>>EXP_A_TXN0.15	[6]

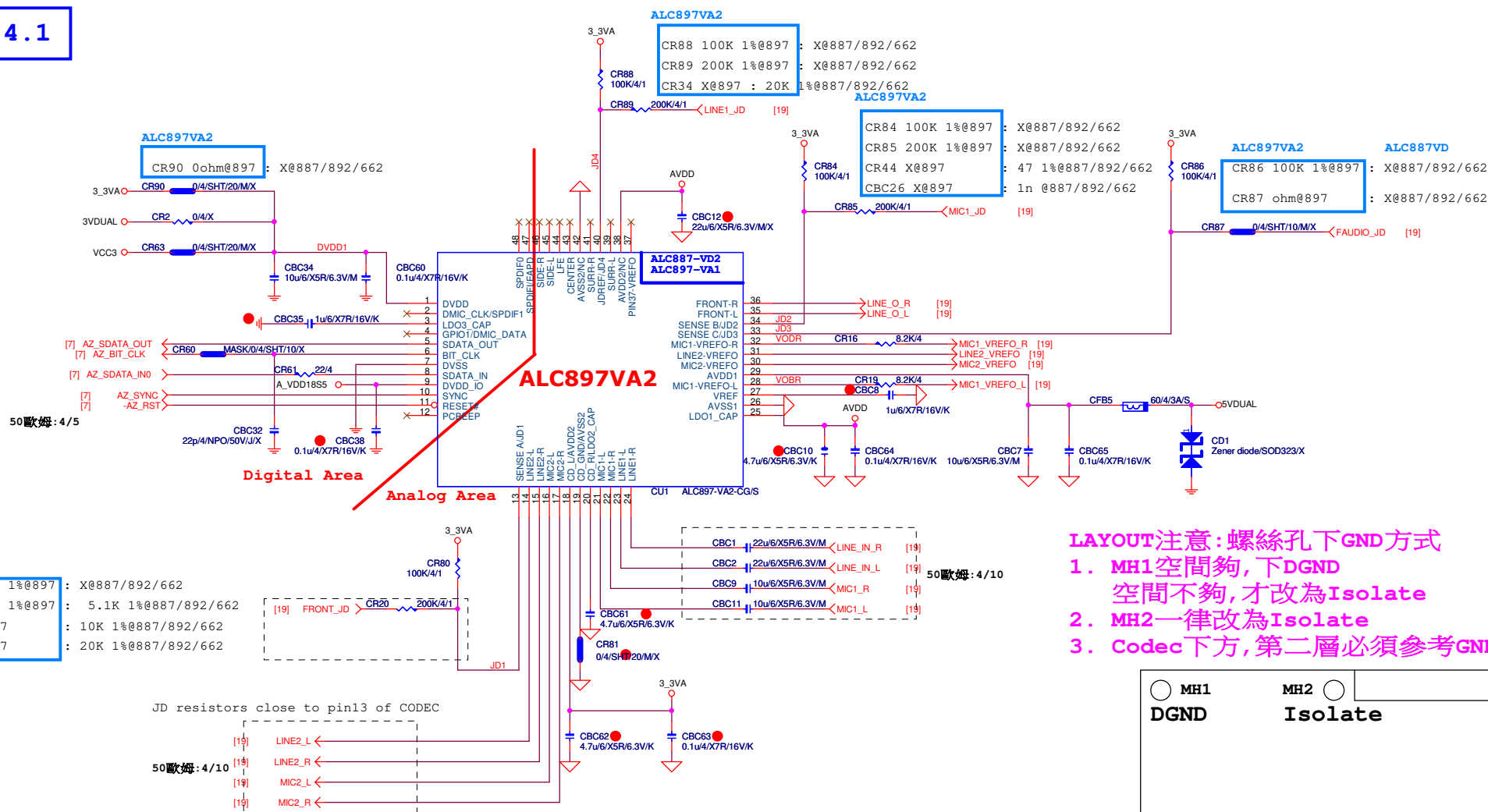
PCIE/16X-164P/BK/LONG DOUBLE

黑色



GIGABYTE™

Title PCI EXPRESS X 16		
Size Custom	Document Number A520M S2H	Rev 1.11
Date Thursday, February 18, 2021	Sheet 17	of 39

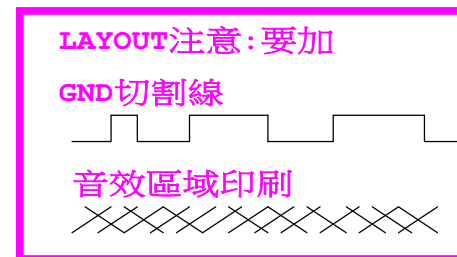


		897	887/892/662
Pin03	LDO3	1uF	10uF
Pin09	DVDD-IO	0.1uF	1uF
Pin18	AVDD2	4.7uF/0.1uF	NC
CR81	AVDD2	0ohm	NC
Pin20	LDO2	4.7uF	NC
Pin25	LDO1	4.7uF	22uF
Pin27	VREF	1uF	10uF
Pin38	AVDD2	NC	22uF

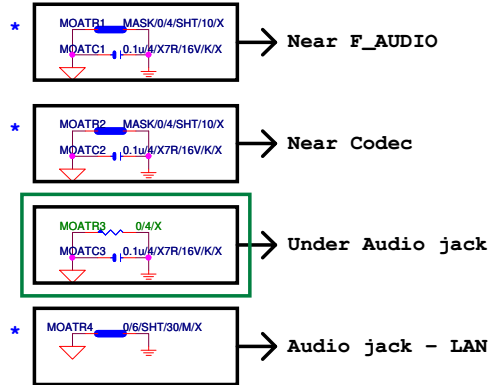
BOM OPTION :

1. Chemicon 音效電容
2. 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

○ MH1	○ MH2
DGND	Isolate

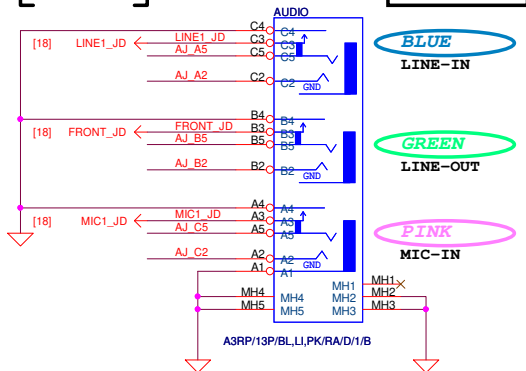
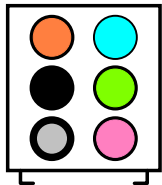


Rev 4.1

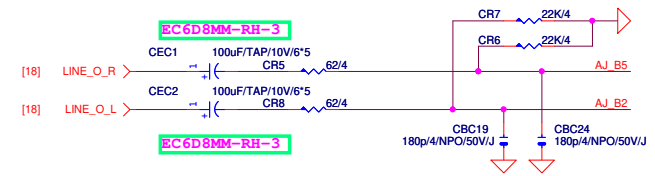


*量産前,MOATR1/MOATR2/MOATR40ohm改short pad

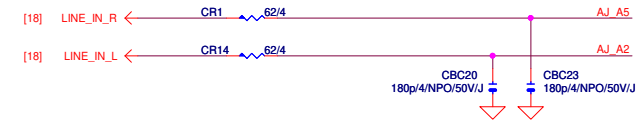
AZALIA JACK



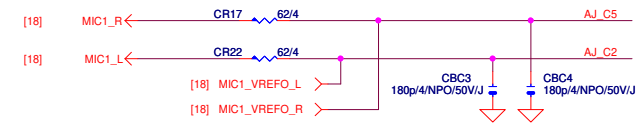
LINE-OUT



LINE-IN



MIC-IN

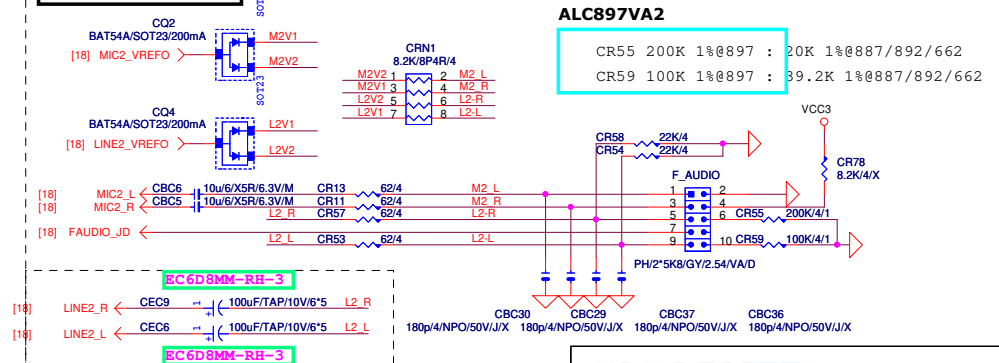


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL



Box header footprint : F_AUDIO

Pin header footprint : F_AUDIO_S

ALC897VA2

CR55 200K 1%@897 : 20K 1%@887/892/662
CR59 100K 1%@897 : 39.2K 1%@887/892/662

GIGABYTE

Title			
AUDIO JACK			
Size	Document Number		Rev
Custom	A520M S2H		1.11
Date:	Thursday, February 18, 2021	Sheet	19 of 39

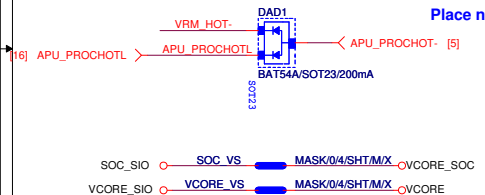
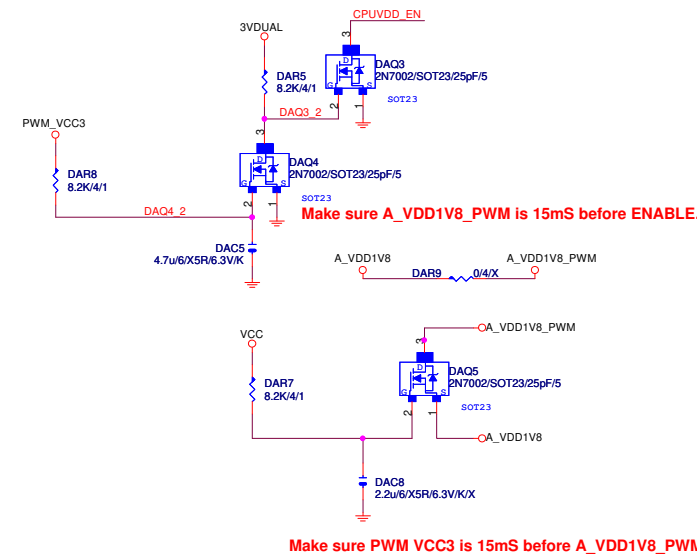
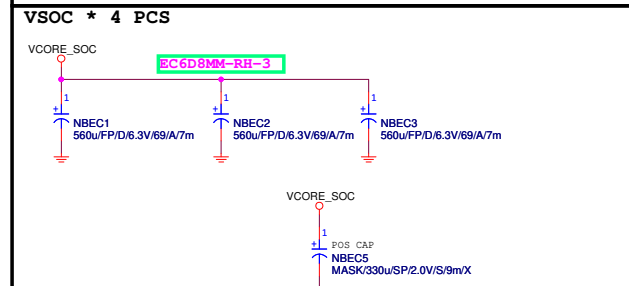
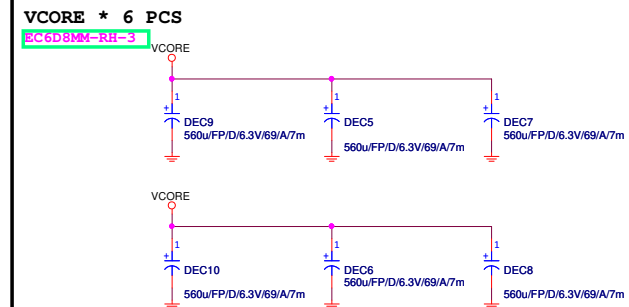
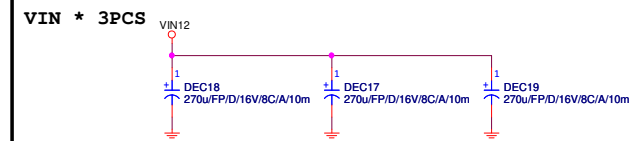
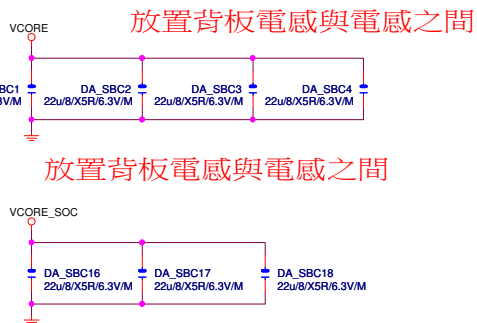
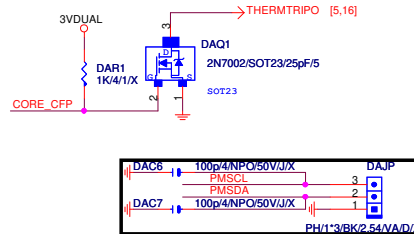
VCC3 DR15 8.2K/4 CPUVDD_EN

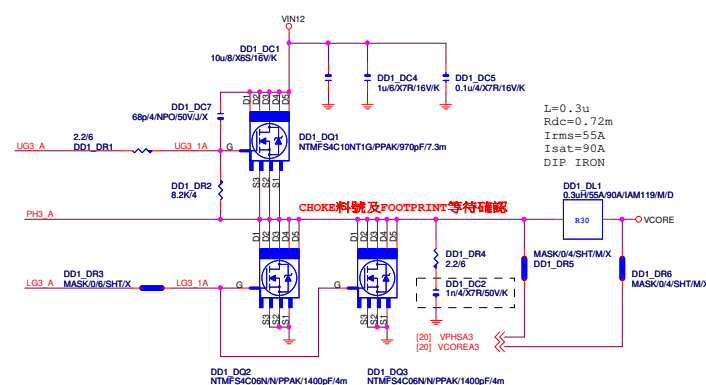
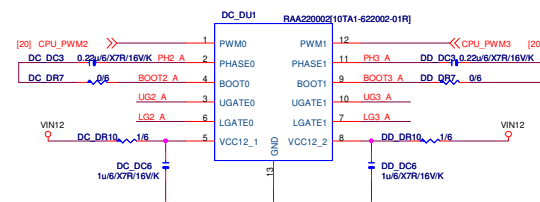
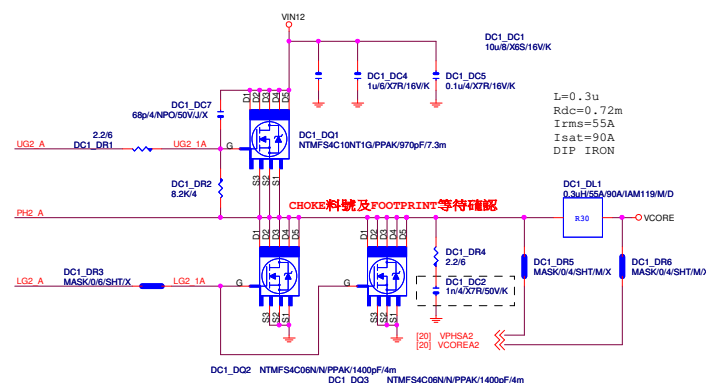
VCC3 DR13 1K/4/1/X VNB_PWOK

VCC3 DR14 8.2K/4 VRM_HOT-

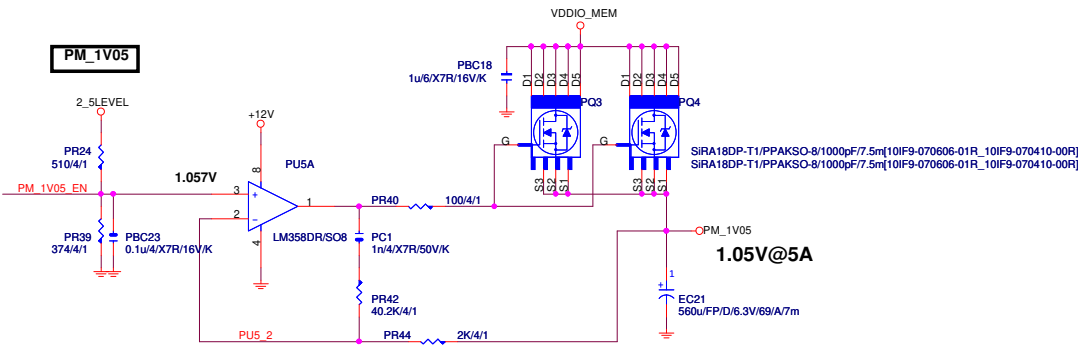
VCC3 DR12 1K/4/1 VR_RDY

DC23 0.1uF/4X7R/16V/K/X

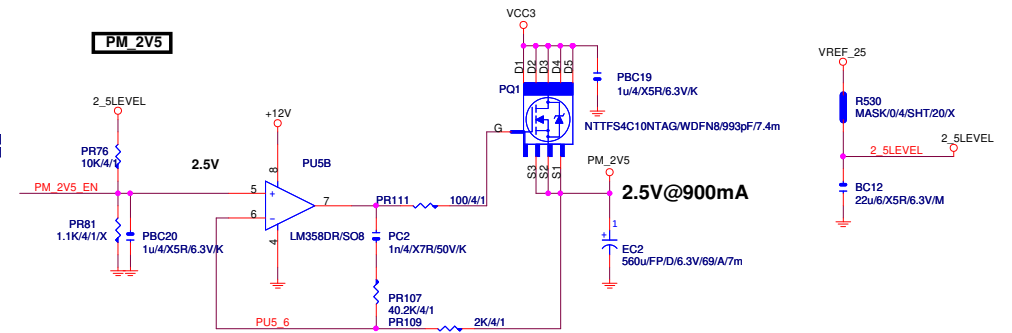
[illegible]



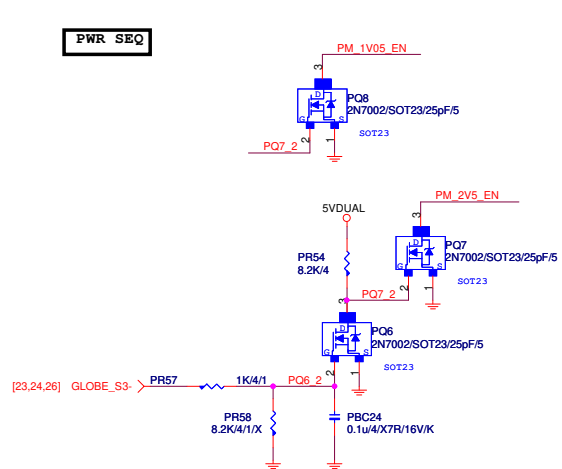
PM_1V05



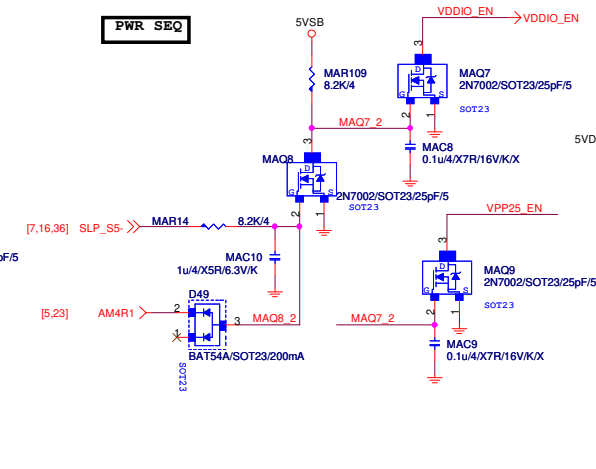
PM_2V5



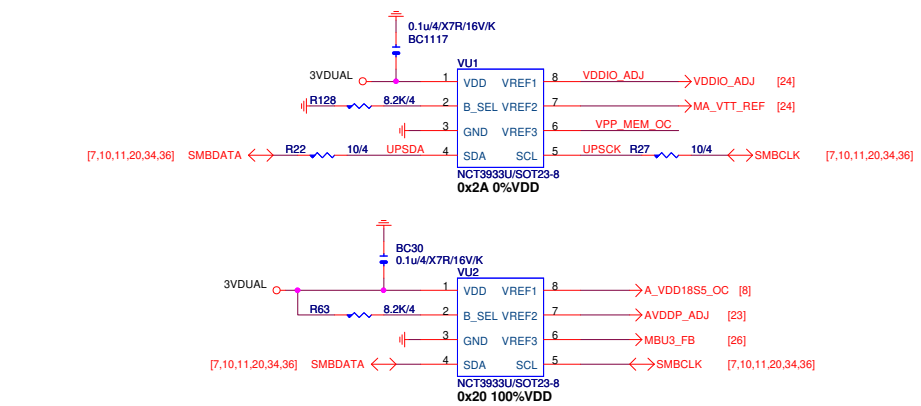
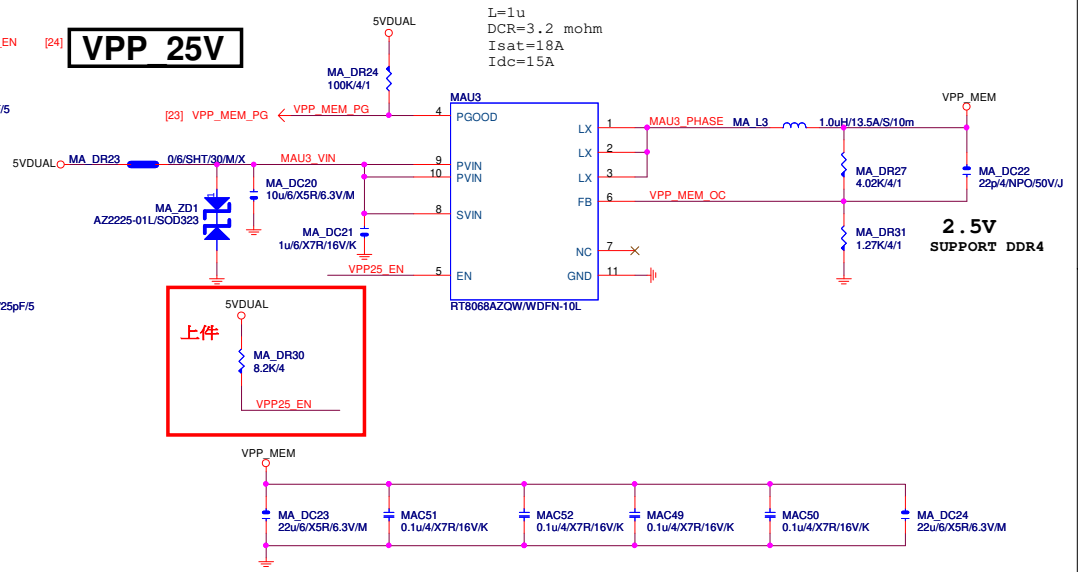
PWR_SEQ



PWR_SEQ



VPP 25V



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

Title

PM POWER

Size Custom

Document Number A520M S2H

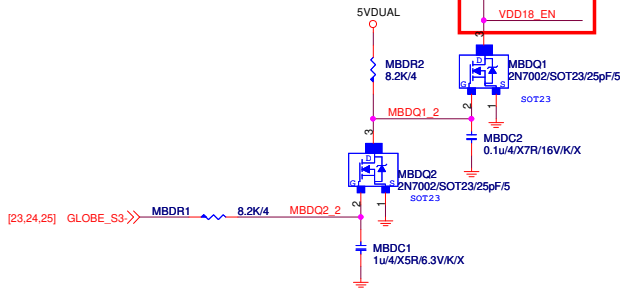
Date: Thursday, February 18, 2021

Rev 1.11

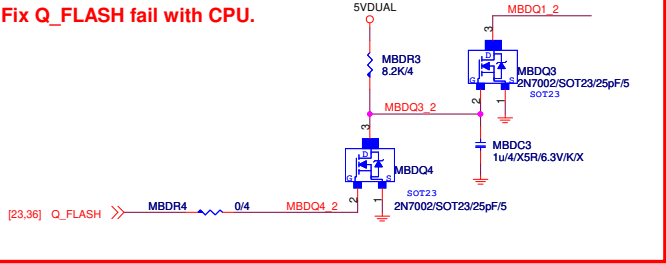
Sheet 25 of 39

PWR_SEQ

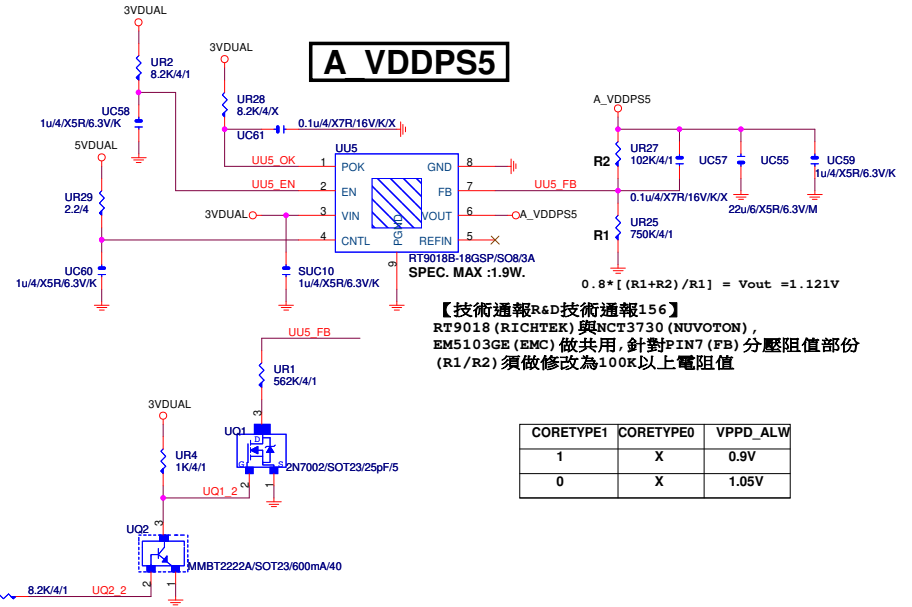
5VDUAL
上件
MB_DR30
8.2K/4
VDD18_EN



Fix Q_FLASH fail with CPU.



A VDDPS5

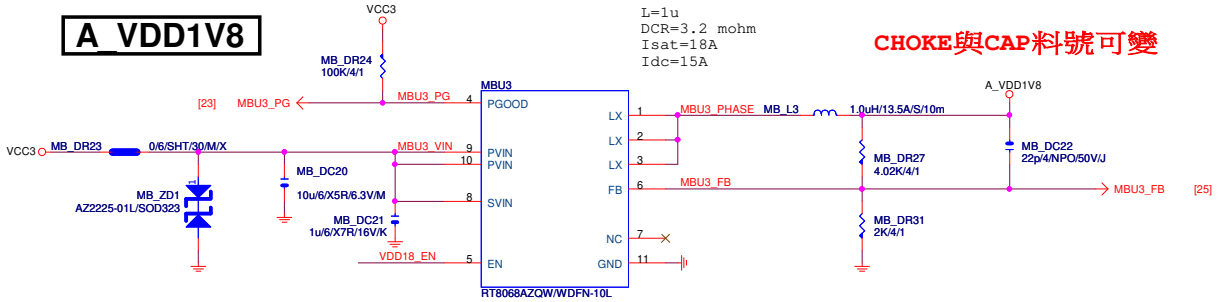


【技術通報R&D技術通報156】
RT9018 (RICHTER) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為 100K 以上電阻值

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

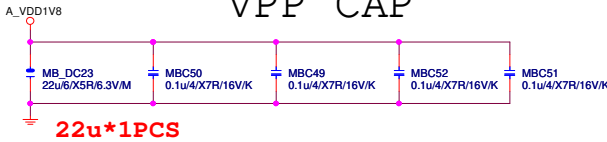
REV:0.4

A VDD1V8

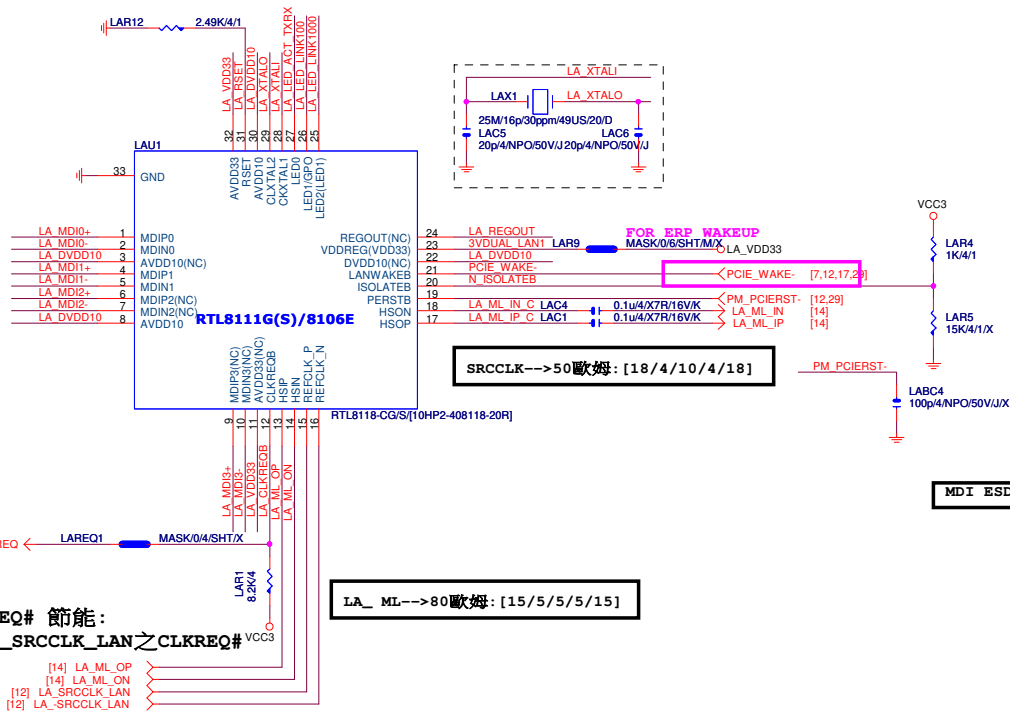


CHOKE與CAP料號可變

VPP CAP

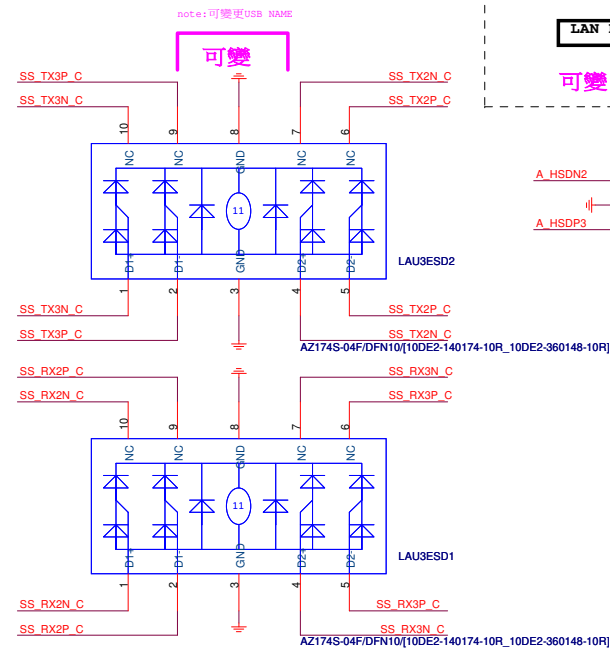
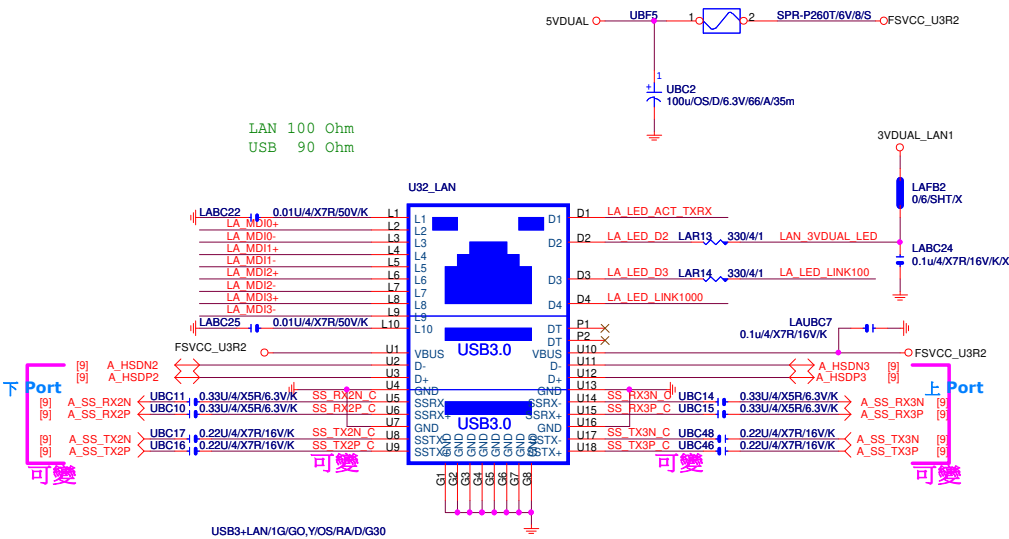


GIGABYTE™		
Title FAN, A_VDD1V8		
Size Custom	Document Number A520M S2H	Rev 1.11
Date: Thursday, February 18, 2021	Sheet 26	of 39

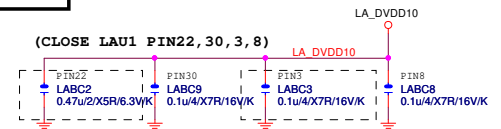


USB_LAN CONNECTOR

note:可變更USB NAME



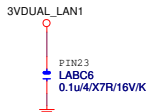
LAN POWER



```
LABC2:1U CLOSE PIN22 [REALTEK REQ]
```

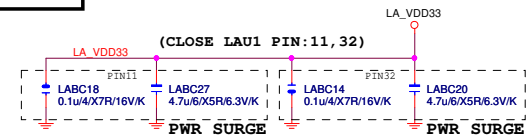
LAN POWER

note: lan power連接及電流



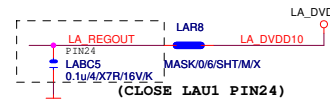
(CLOSE LAU1 PIN23)

LAN POWER



```
LABC18,27:CLOSE PIN11[REALTEK SURGE]
LABC14,20:CLOSE PIN32[REALTEK SURGE]
```

LAN POWER

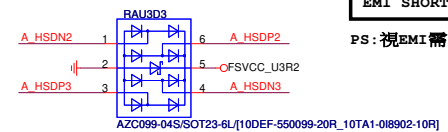


LAN POWER

note: lan power連接及電流

For PVT :LAPW1 改 R0402-2-SHORT20

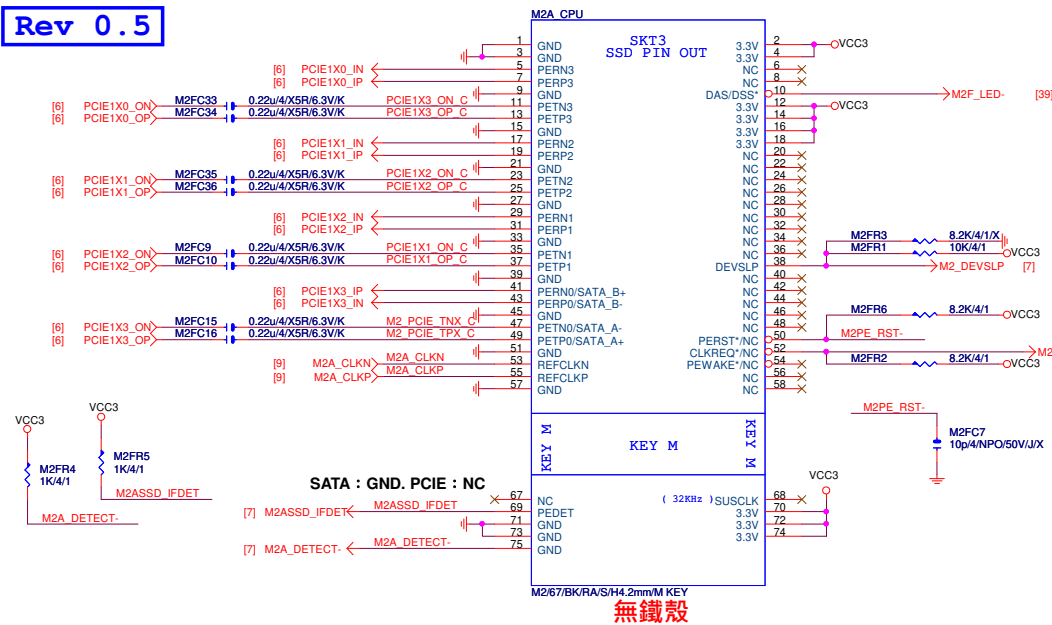
可變



EMI SHORT PAD

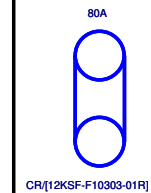
PS:視EMI需求

Rev 0.5



Footprint : NGFF-M-75P-8CM-09MM-SMD

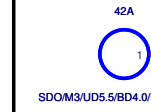
DIP螺柱



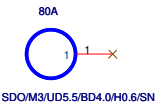
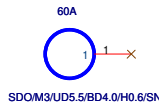
80A



SMD螺柱



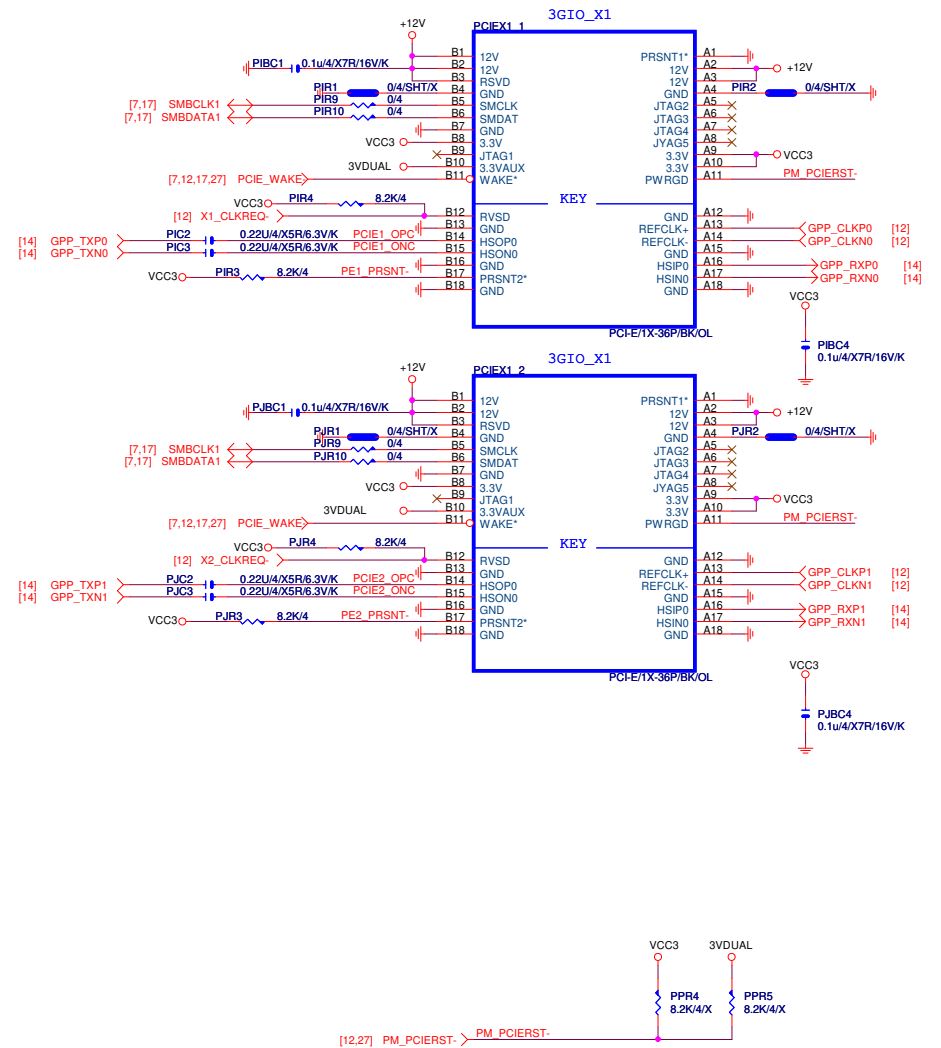
10KS2-040131-02R



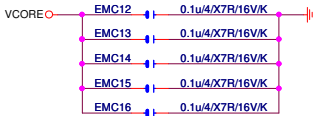
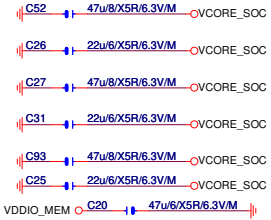
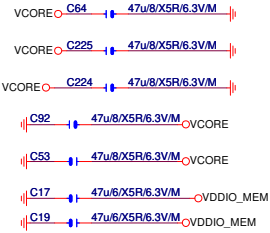
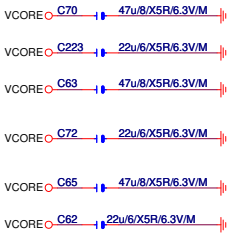
★ Footprint : HOLE_C236D165-A

GIGABYTE™

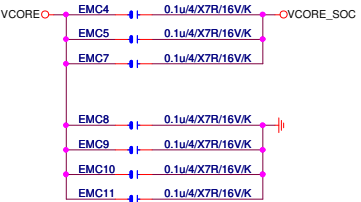
Title			U.2, M.2 SOCKET
Size	Document Number	Rev	
Custom	A520M S2H	1.11	
Date:	Thursday, February 18, 2021	Sheet	28 of 39



CPU TOP CAVITY



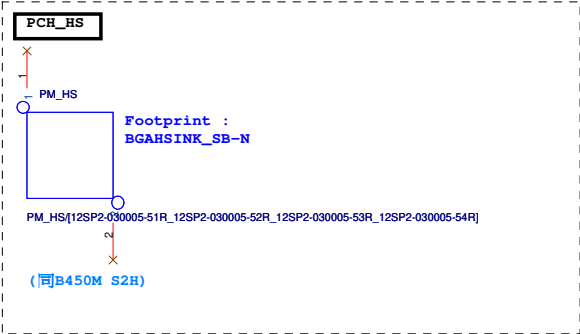
Cross Plane CAP



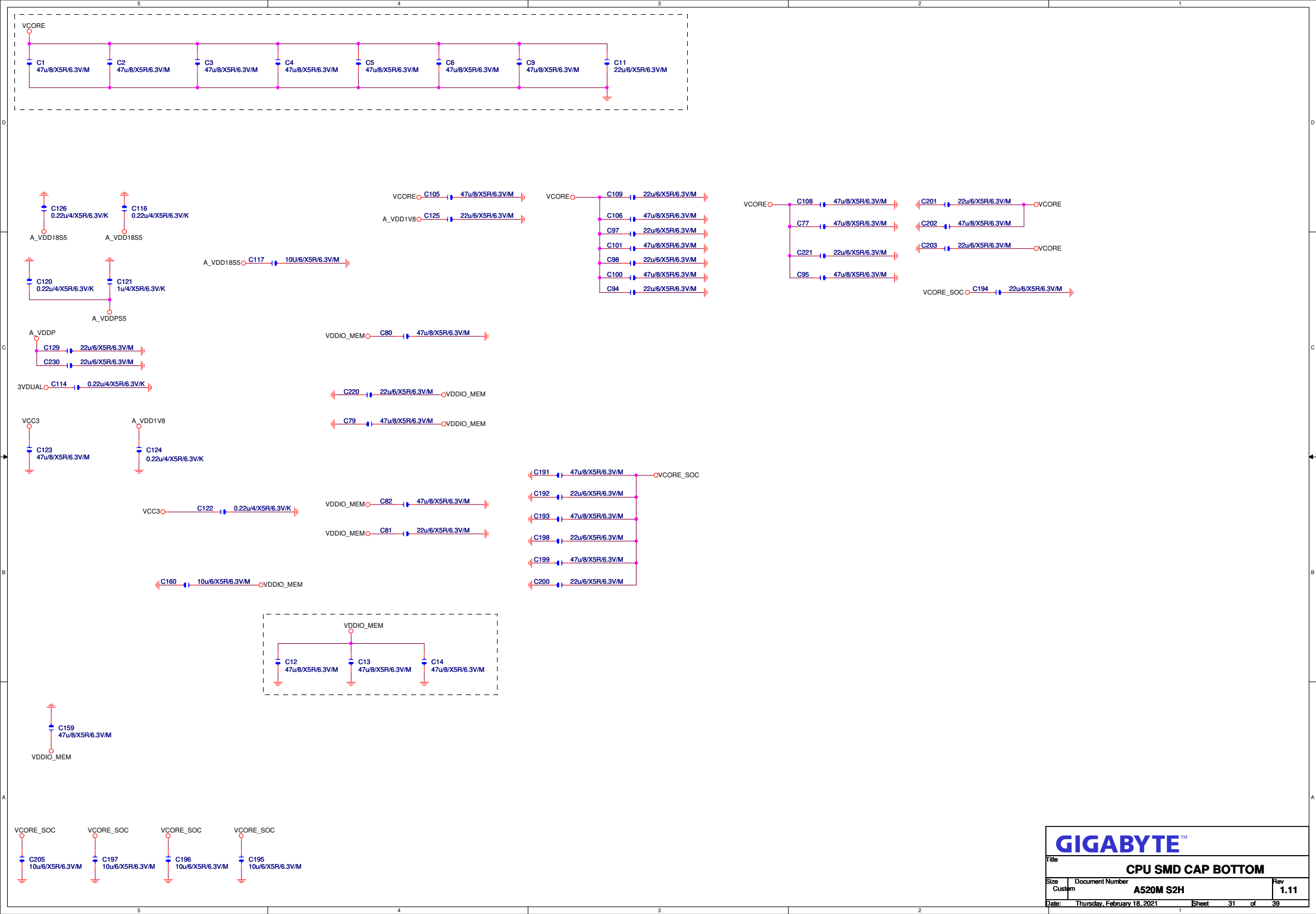
Cross Plane CAP

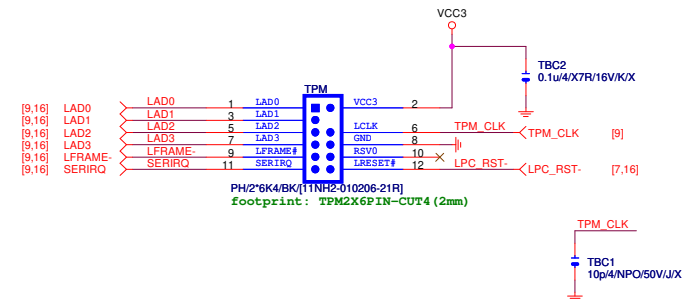


裝甲HEATSINK 分成五大部份

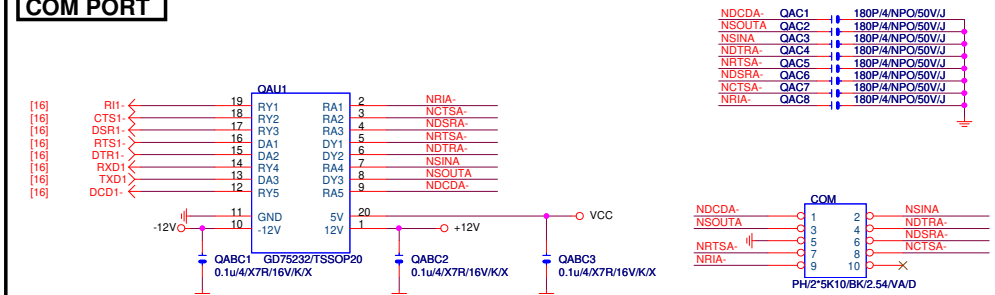


- * PCB顏色 : 咖啡黑
- * 文字面 : 灰色
- * 圖騰 : 同B450M S2H





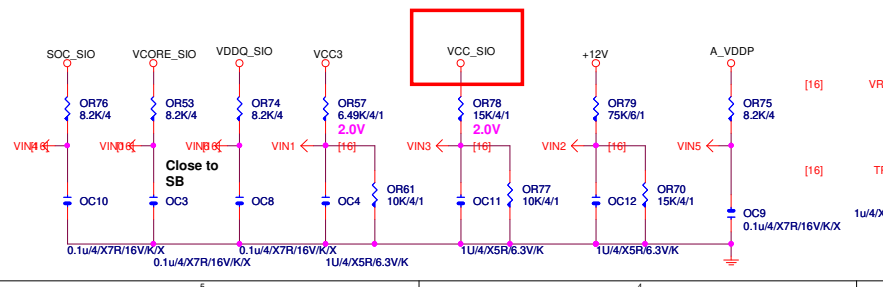
COM PORT



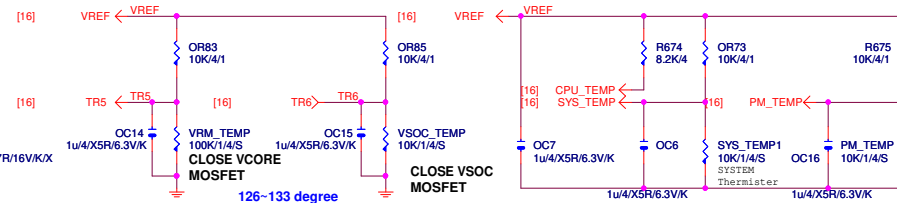
LPT PORT

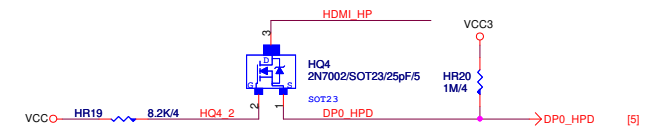
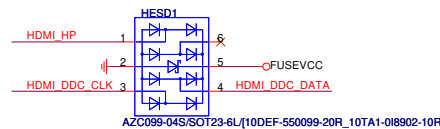
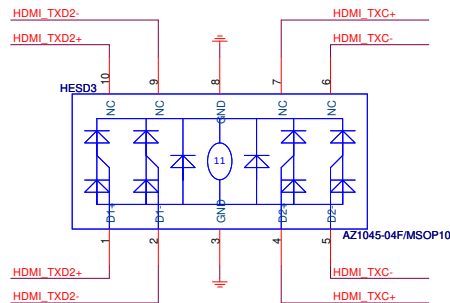
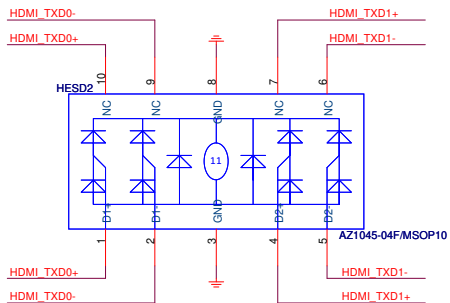
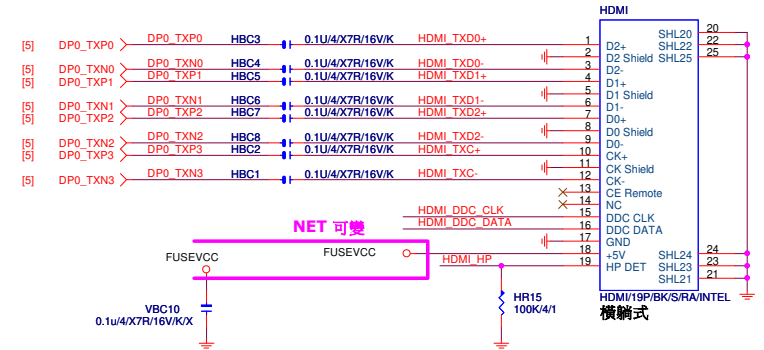
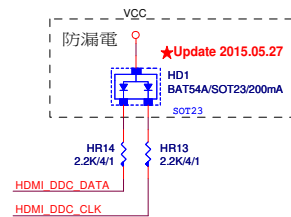
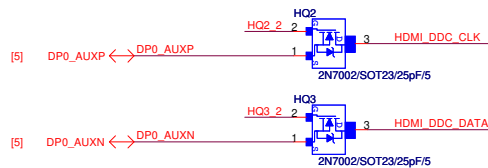
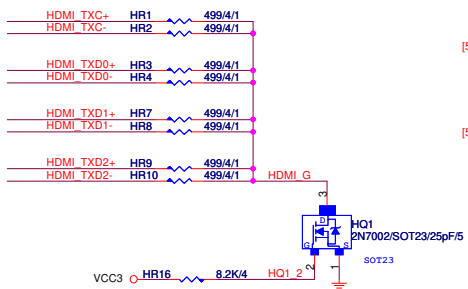


Rev: 0.6



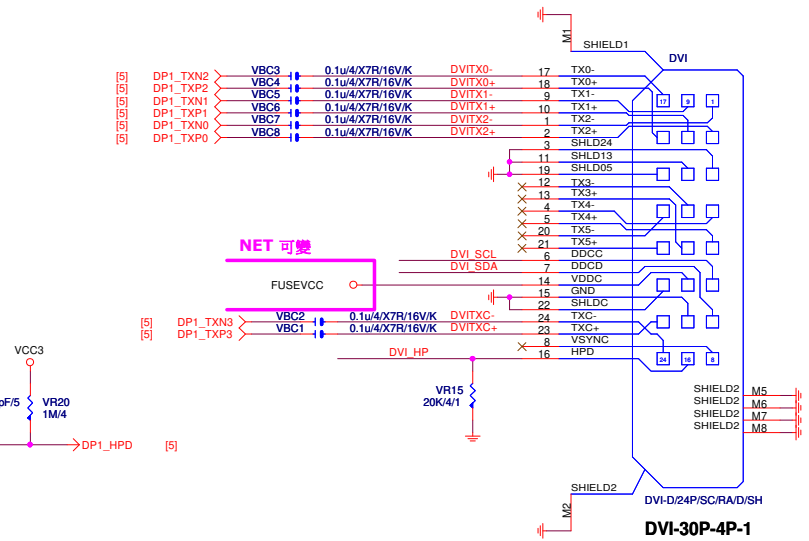
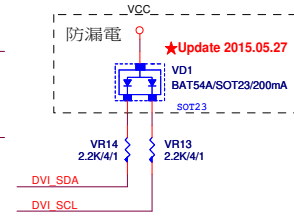
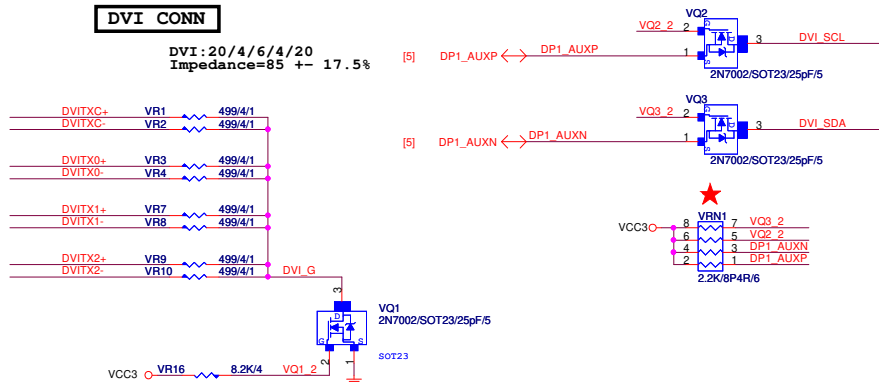
Hardware Monitor circuits - Temperature



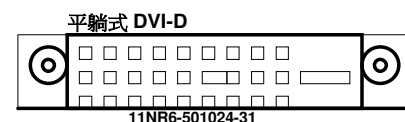
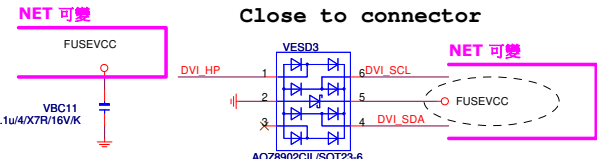
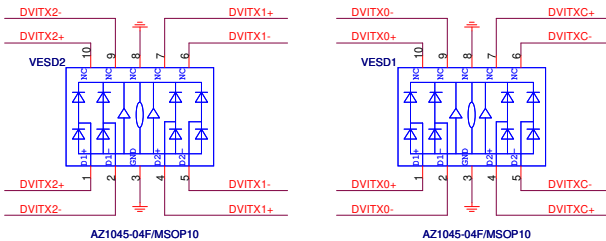


DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector



GIGABYTE

Title: **HDMI,DVI**

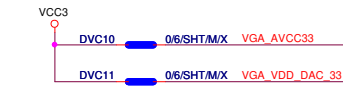
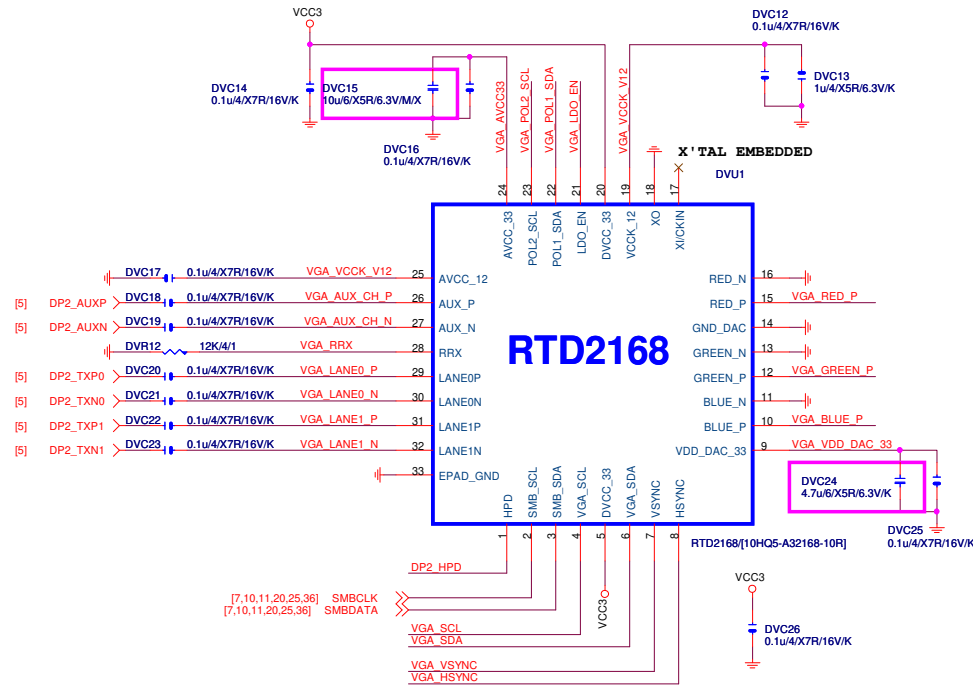
Size: Custom

Document Number: **A520M S2H**

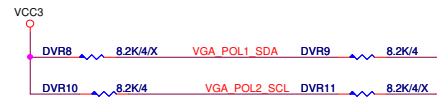
Date: Thursday, February 18, 2021

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Rev: **1.11**



Power on latch



POL2_SCL (PIN23)	POL1_SDA(PIN22)	
	0	1
0	X	EP MODE
1	ROM ONLY MODE	EEPROM MODE

Embedded LDO



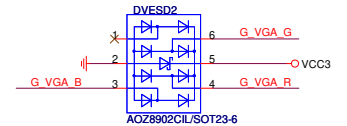
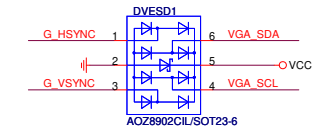
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD

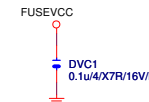
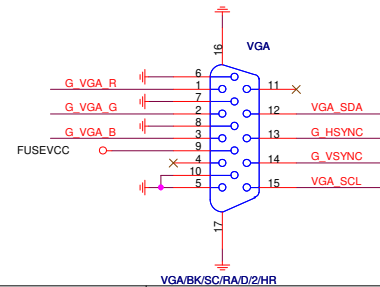


Gigabyte Technology

VGA ESD



架高型VGA (BLACK)
Footprint : VGACONN-DH-2

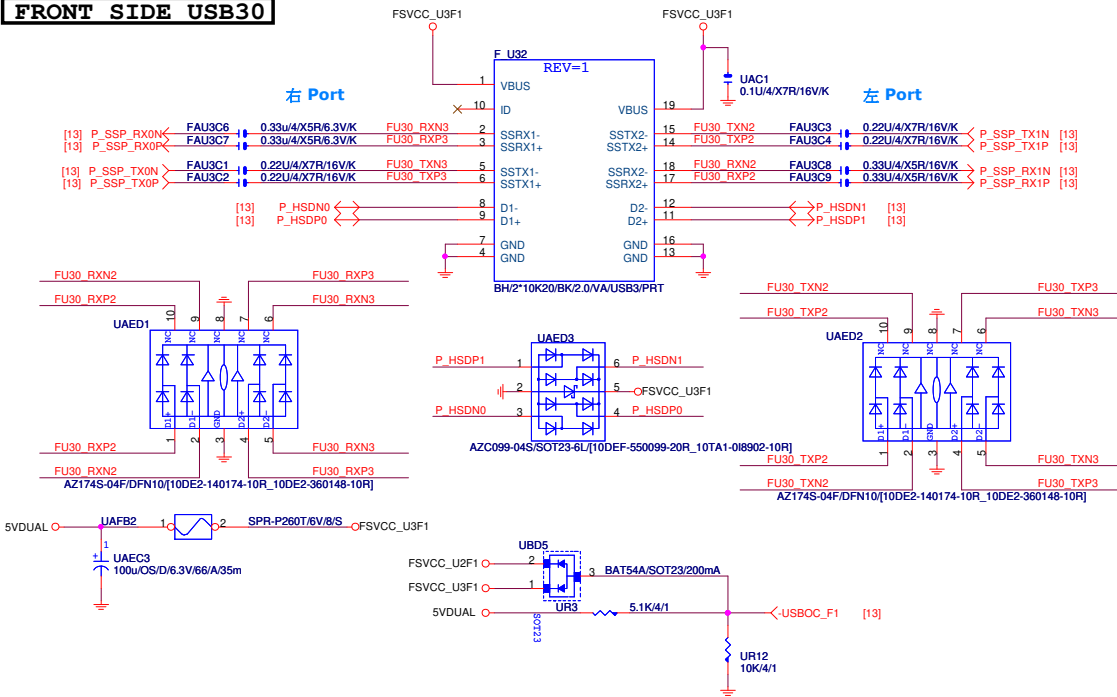


GIGABYTE™			
Title			
VGA			
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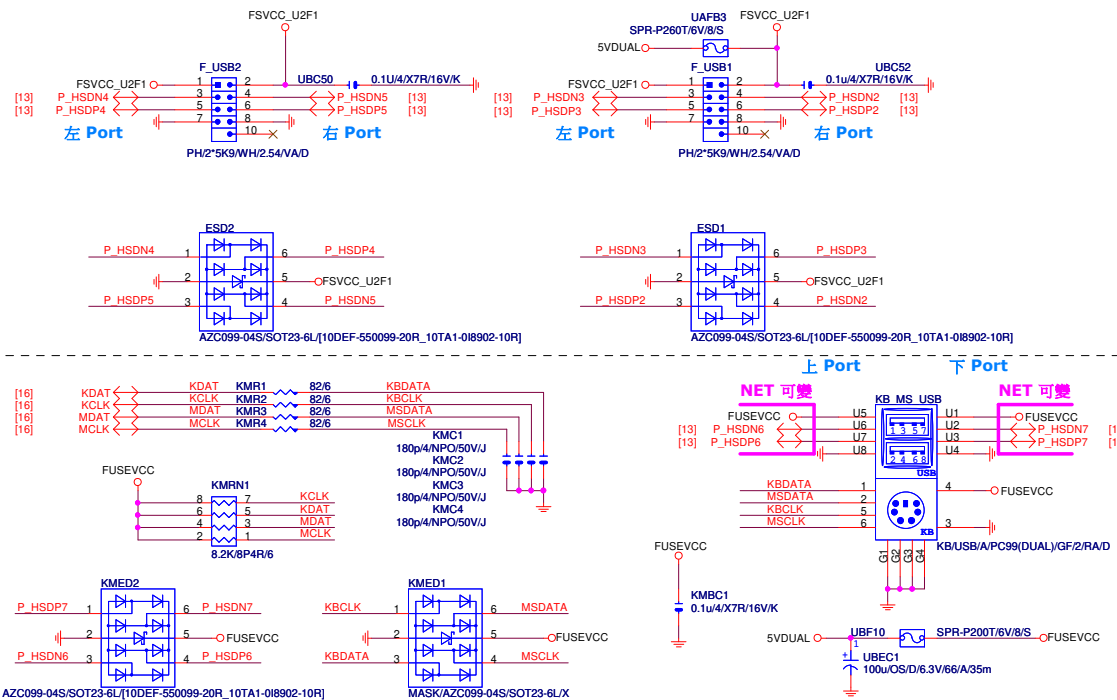
Close to Filter

FOR EMI

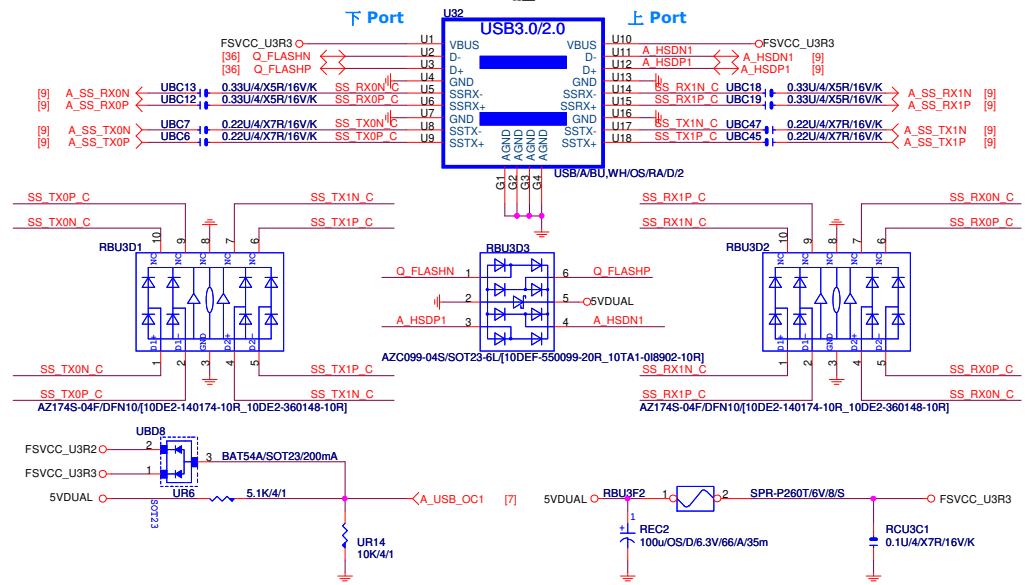
FRONT SIDE USB30



FRONT SIDE USB2.0

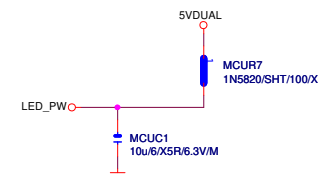
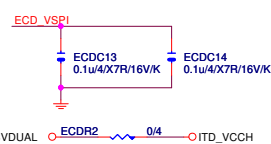
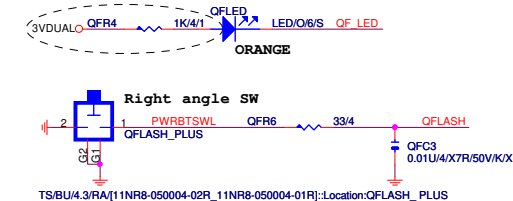
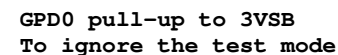
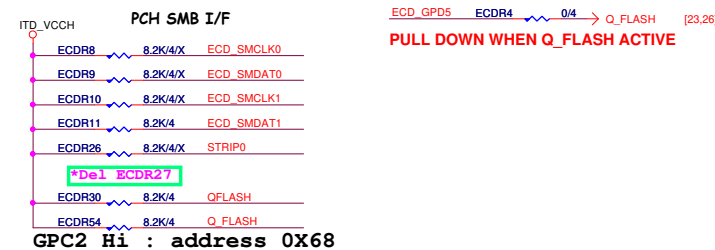


FROM CPU WITH Q_FALSH



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F_USB ,F_USB30 ,R_USB30 , KB_MS USB			
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第三區 LED

第三區 LED CONTROL

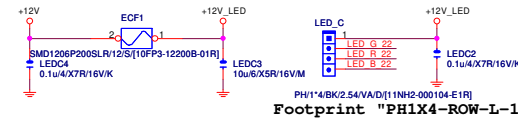
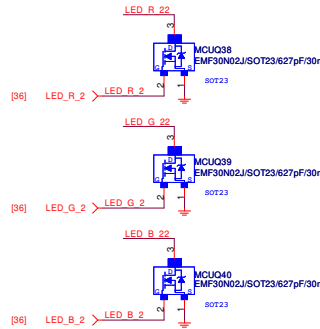
第五區 LED

第二區 LED CONTROL

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)

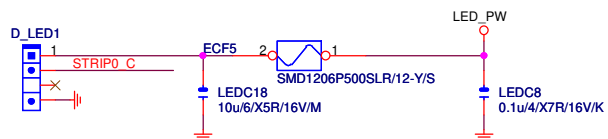
燈條 LED (LED_C2放在PCB右邊板邊位置)



第四區 LED

第六區 LED (靠近左上板邊位置)

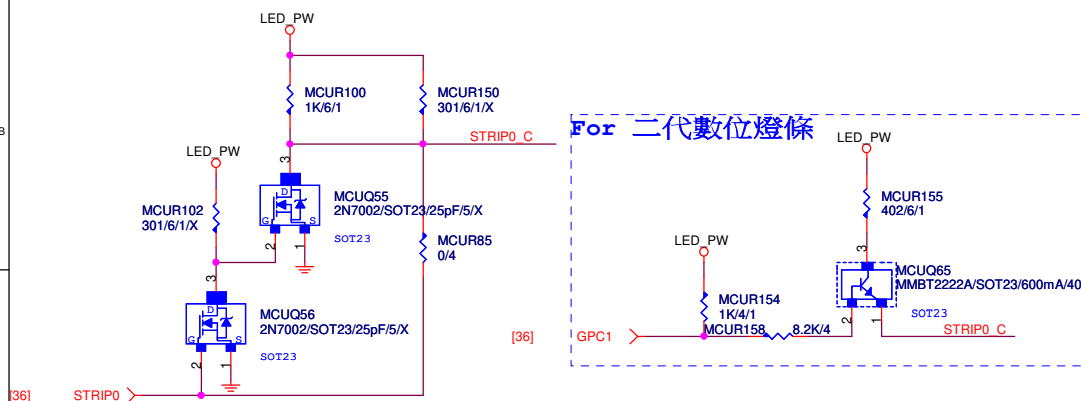
Digital LED Strip1



PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint PH1X4-CUT3-LED-L

燈條 Level shift



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D_LED

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